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TEMPO
Technologies and hardware for neuromorphic computing

Deliverable

D5.6 – European Neuromorphic Hardware Roadmap

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1. Publishable summary

In this document, we will first report on a deeper contamination investigation which was part of Task 5.2. This additional activity was accepted in the third amendment, and it was also decided to report all the results in the present deliverable. This work was jointly performed by CEA and FhG-IPMS using CEA facilities. An FhG-IPMS PhD student, supervised by both parties, spent 4 months in CEA's cleanroom running lots with intentional and controlled Li contamination, and performed their characterization and analyses. The result of this work is reported in section 3 of this document.

The main objective of deliverable D5.6 is to define a neuromorphic hardware roadmap and is the result of Task 5.3 (RTO synchronization). To arrive at this roadmap, this deliverable first provides a comparative analysis of the outcomes from the different work packages within TEMPO, covering the levels between eNVM technologies (WP2), circuit design and architecture (WP4) and applications (WP6). On each of these three levels, a benchmarking table is provided with appropriately chosen KPIs. From these benchmarking tables, overall conclusions are drawn connecting technology to applications. These conclusions lead to a gap analysis, which will define a roadmap definition for the different eNVM technologies represented within TEMPO.

Important to note is that the benchmarking approach is fully in line with the approach taken in the EU-project ANDANTE, ensuring continuity and consistency between TEMPO and ANDANTE. Furthermore, the roadmap described at the end of this document has been very useful for the TEF project.