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TEMPO
Technologies and hardware for neuromorphic computing

Deliverable

D6.6 – Chip dicing: packaging and board bringup: Ferro

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1. Publishable summary

Deliverable D6.6 reports the successful fabrication and bring-up of the evaluation board of several integrated circuit designs for analog in-memory computing of Fraunhofer IIS and Fraunhofer EMFT, designed and fabricated in 28SLPe GlobalFoundries technology.

The designed 9 mm^2 ASIC contains the following circuits:

- 3 analog fully connected layers based on SRAM synaptic weights with 7 levels to perform inference and SRAM and FeFET test layers
- An SRAM-based current-steering crossbar; a FeFET-based crossbar with flexible output precision and calibration; a 110 MHz GBW fully differential amplifier with a CMFB and AB-Bias using a cascaded control loop; a –2.5 V to 3.6 V bipolar charge pump; a level shifter using a proposed structure allows bi-directional voltage shifting.

A design for test, test plans and test scripts have been developed to properly test the functionality and performance of the building blocks of the analog in-memory computing circuits.