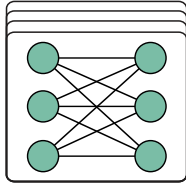




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# TEMPO

Technologies and hardware for neuromorphic computing

## Deliverable

### D3.15 – STT-MRAM Mbit array validation

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## 1. Publishable summary

In this document, imec is reporting performance analysis of the STT-MRAM characterization array that was built during the TEMPO project. The array is targeting ~ 45nm diameter STT-MRAM pillars at a pitch of 200nm. The frontend logic transistors are fabricated on GlobalFoundries 40nm process node and the MRAM specific module is integrated in imec. Overall, we see good distributions for the key figures of merit of the technology. Importantly, we see that the issues faced in the past (series resistances, defectivity) have been resolved. These results will be also enablers for the ongoing ANDANTE project.