This project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 826655. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Belgium, France, Germany, Netherlands, Switzerland

Addressing the call/topic: H2020 ECSEL-2018-2-RIA
Research and Innovation Action

TEMPO
Technologies and hardware for neuromorphic computing

Deliverable

D3.11 – Base wafer finishing with Ferroelectric Memory

Work Package:	WP3 (Integration)
Dissemination level:	Confidential
Official due date:	30.06.2022
Document editor:	Thomas Kämpfe (Fraunhofer)
Contributing partners:	FhG
Internal reviewers:	Ilja Ocket(IMEC), Björn Debaillie(IMEC), Gabriel Pares (CEA)
Document version:	V1.0

1. Publishable summary

This report describes, and demonstrates an alternative approach of integrating 1T-1C FeFET having a separated transistor (1T) without modifying front-end CMOS technology and an additional gate-coupled ferroelectric (FE) capacitor (1C) embedded in the interconnect layers. Starting from the results of FE capacitor integration and 1T-1C single cell characterization, this report describes the realization and obtained results of a fully integrated 8 kbit memory array implementation.