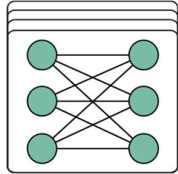




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1. Publishable summary

This report describes, and demonstrates an alternative approach of integrating 1T-1C FeFET having a separated transistor (1T) without modifying front-end CMOS technology and an additional gate-coupled ferroelectric (FE) capacitor (1C) embedded in the interconnect layers. Starting from the results of FE capacitor integration and 1T-1C single cell characterization, this report describes the realization and obtained results of a fully integrated 8 kbit memory array implementation.