This project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 826655. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Belgium, France, Germany, Netherlands, Switzerland

Addressing the call/topic: H2020 ECSEL-2018-2-RIA
Research and Innovation Action

TEMPO
Technologies and hardware for neuromorphic computing

Deliverable

D3.9 – Compact model generation for BEoL FeFET

Work Package:	WP3 (Integration)
Dissemination level:	Confidential
Official due date:	30.04.2022
Document editor:	Thomas Kämpfe (FhG)
Contributing partners:	FhG
Internal reviewers:	Ilja Ocket (IMEC), Björn Debaillie (IMEC)
Document version:	V1

1. Publishable summary

This report describes various compact model card extractions for FeFET based on measurements and calibration. The FeFET compact models (e.g. Preisach model, Jiles-Atherton model) was developed at Fraunhofer IPMS and the Jiles-Atherton model is going to be published (accepted for publication at SISPAD).
Typical behaviour is described by one model card by calibration with IDVD and IDVG measurements. To account for variability, the users can use a Monte Carlo model card which includes statistical variation of the threshold voltage. Performing SPICE pseudo random simulations, experimental transconductance curves can be reproduced.