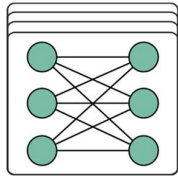




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# TEMPO

Technologies and hardware for neuromorphic computing

## Deliverable

### D3.9 – Compact model generation for BEoL FeFET

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## 1. Publishable summary

This report describes various compact model card extractions for FeFET based on measurements and calibration. The FeFET compact models (e.g. Preisach model, Jiles-Atherton model) was developed at Fraunhofer IPMS and the Jiles-Atherton model is going to be published (accepted for publication at SISPAD).

Typical behaviour is described by one model card by calibration with IDVD and IDVG measurements. To account for variability, the users can use a Monte Carlo model card which includes statistical variation of the threshold voltage. Performing SPICE pseudo random simulations, experimental transconductance curves can be reproduced.