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Deliverable

D3.14 – Base wafer finishing process flow improvements for OxRAM

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1. Publishable summary

This report describes complementary work after the D3.12 report related to the process development done at CEA to finish the 28nm base wafers with OxRAM memory cells to implement the specific neuromorphic circuits (LARGO) designed in WP4.

Process modules were developed from a new mask-set named MAD303, using full 193nm immersion lithography, leading to main features sizes of 100nm VIAinf, 90nm VIAsup and ~80nm spacing between PTMEM dots after SiN capping in order to fabricate OxRAM shrunken bitcells in 300mm. The development of this OxRAM module was already reported in D3.12.

This report pushes the development of the OxRAM process flow, addressing the following objectives:

- Complete the original planned integration for complex neuromorphic circuits by adding routing capability over memory arrays.
- Assess process capability and identify the limitations towards shrunken bitcells integration to study the scalabity of OxRAM at bitcell level for future tape-out.

Process optimization of the OxRAM technology conducted in the frame of this report comprises:

- Process optimization and integration of a two metallization levels interconnect using dual damascene copper on top of memory for complex circuits enablement.
- Study the patterning process for shrunken ptmem dots and demonstration of even smaller size present in the design. Limitation of the current process integration will be characterized with physical analysis.

Basic electrical characterizations on the full flow lot are also presented that demonstrates the functionality of the OxRAM technology inserted in the FD28 CMOS BEOL.