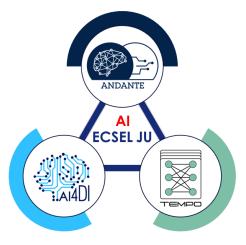
International Workshop on Embedded Artificial Intelligence Devices, Systems, and Industrial Applications (EAI)



ECSEL JL

Milan, Italy 19 September 2022

International Workshop on Embedded Artificial Intelligence Devices, Systems, and Industrial Applications (EAI)



Low-Power Vertically Stacked One Time Programmable Multi-bit IGZO-Based BEOL Compatible Ferroelectric TFT Memory Devices with Lifelong Retention for Monolithic 3D-Inference Engine Applications





19 September 2022 Milan, Italy



- Introduction
- Process flow
- Capacitor Characterization
- Transistor Characterization
- Implications to Neural Network
- Benchmarking

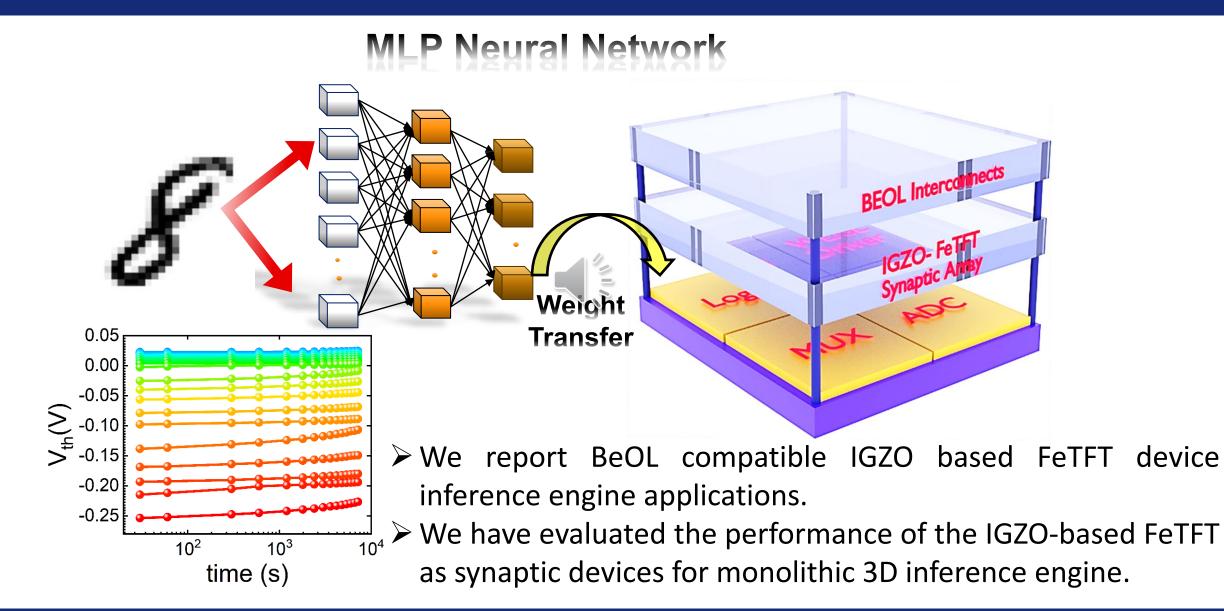
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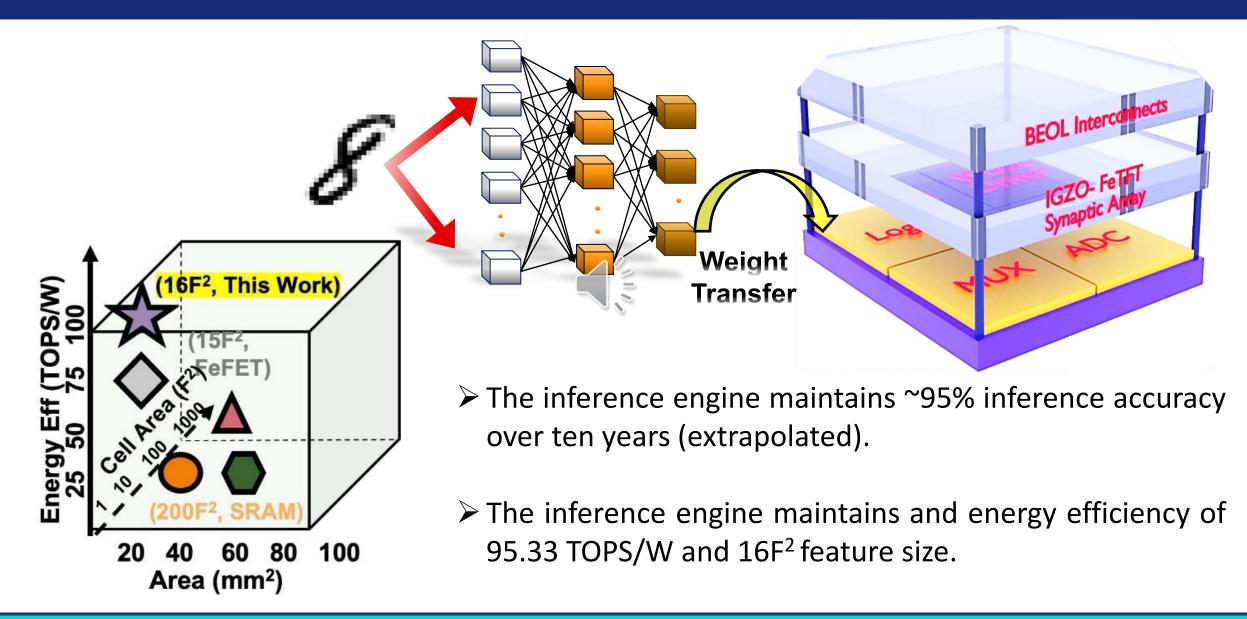
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Introduction



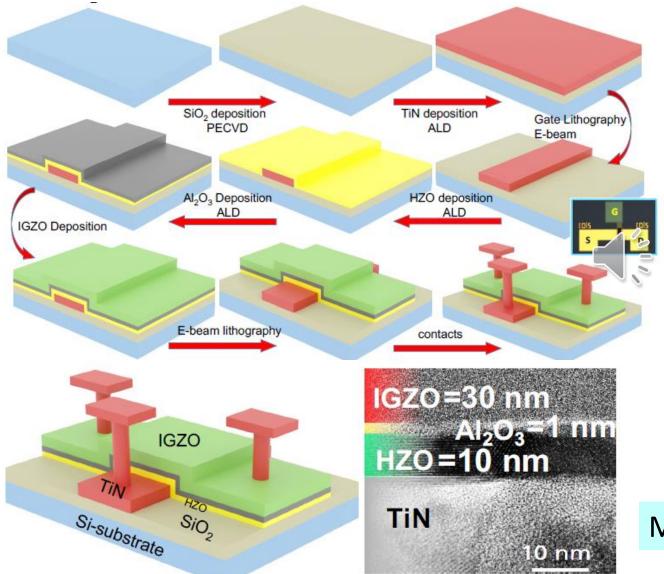
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Process flow



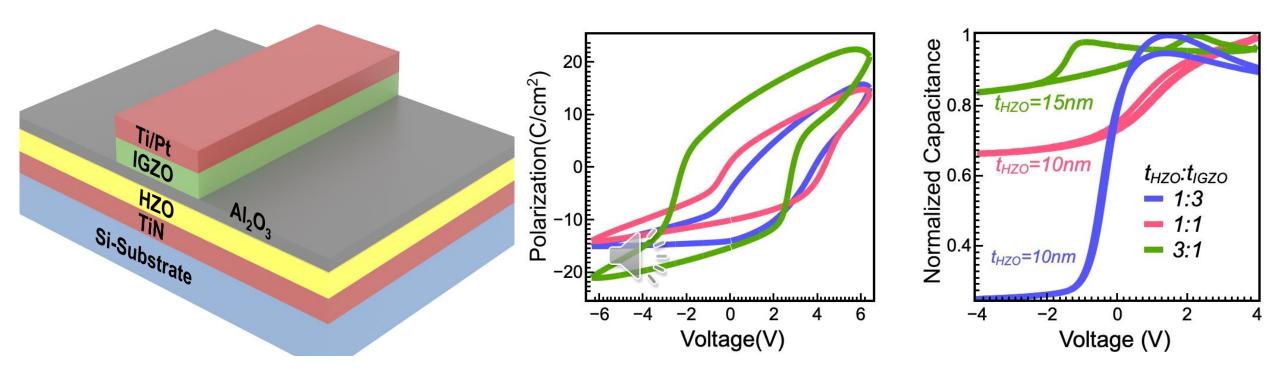
Standard cleaning of Si wafer Deposition of SiO₂ by PECVD Deposition of TiN by ALD Gate lithography by E-beam Deposition of HZO by ALD Deposition of Al₂O₃ by ALD **Deposition of IGZO** E-beam lithography Contact pad deposition.

Maximum process temperature is 350°C



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Capacitor Characterization



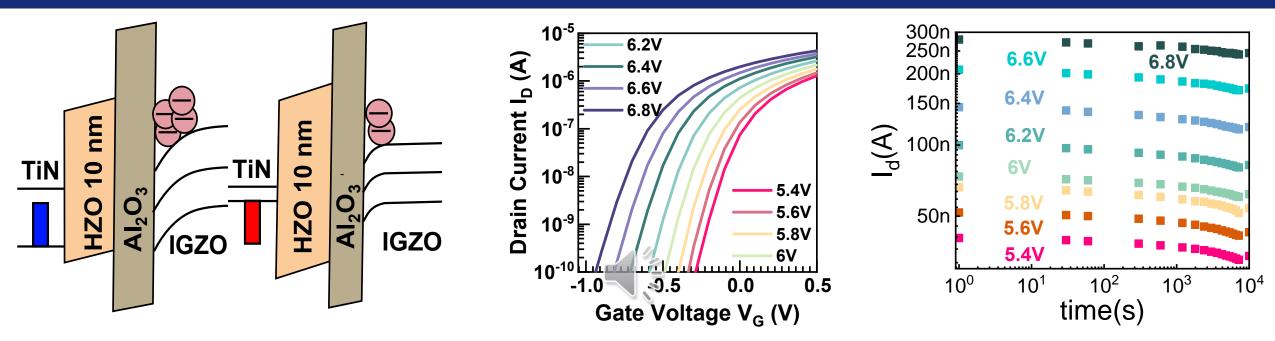
Schematic of the gate-stack with IGZO as semiconductor and HZO as a ferroelectric layer.
Polarization versus voltage (P–V) response of metal-semiconductor-FE-metal (MSFM) gate stacks with various thicknesses of the HZO and IGZO.

Capacitance versus voltage (C–V) response of metal-semiconductor-FE-metal (MSFM) gate stacks with various thicknesses of the HZO and IGZO.



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Transistor Characterization

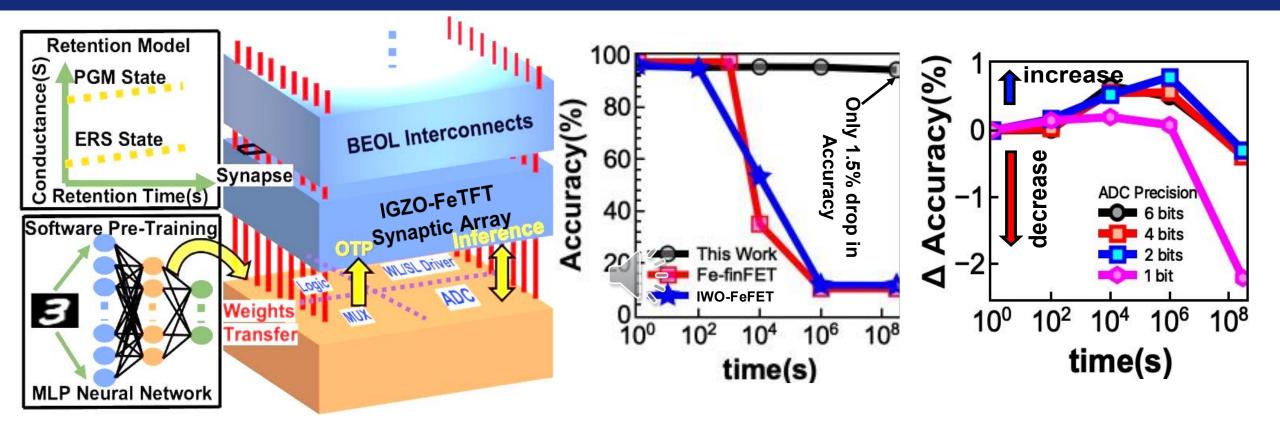


- > The band diagram of the IGZO-MOS capacitor during the program and erase operation. Although the high value of μ_n facilitates fast programming, the low value of μ_p inhibits the erase operation by preventing the supply of holes during erase operation.
- ➤ 3 bits/ cell WRITE operation in IGZO-based FeTFTs with 200 ns wide pulses of minimum amplitude 5.2 V and maximum amplitude of 6.8 V.
- The measured retention characteristics show stable retention of 8-states for 10⁴ seconds and for ten years for 2bits/cell operation with negligible degradation.



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Implications to Neural Network

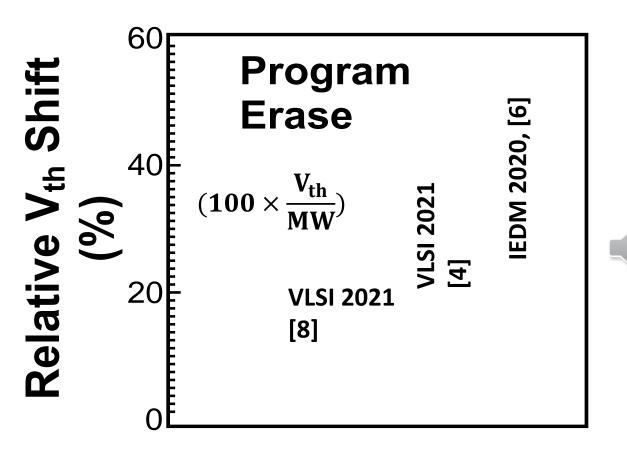


- > The modus operandi of monolithic 3D inference engine based on multilayer perceptron neural network.
- The reported inference engine shows life-long lossless inference operation and (c). Reducing the ADC precision to 1bit causes a mere accuracy degradation of 1.87% from FP precision.
- > 1-bit ADC shows less than 2% accuracy loss over 10 years.



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Benchmarking



Device Type	Fe-FinFET [9]	IWO-FeFET [14]	This Work
M3D Integrator	No	Yes	Yes
Cell Area (F ²)	15F ²	15F ²	16F ²
	100K	4M	100M
MW @10 years	1	0.2	1
Inference Accuracy Drop @10 years	~85%	85%	1.5%
Energy Efficiency (TOPS/W)	N/A	71.04	95.33 (Binary)

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Event Organisers









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