International Workshop on Embedded Artificial Intelligence Devices, Systems, and Industrial Applications (EAI)

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AI
ECSEL JU

Low-Power Analog In-memory Computing Neuromorphic Circuits

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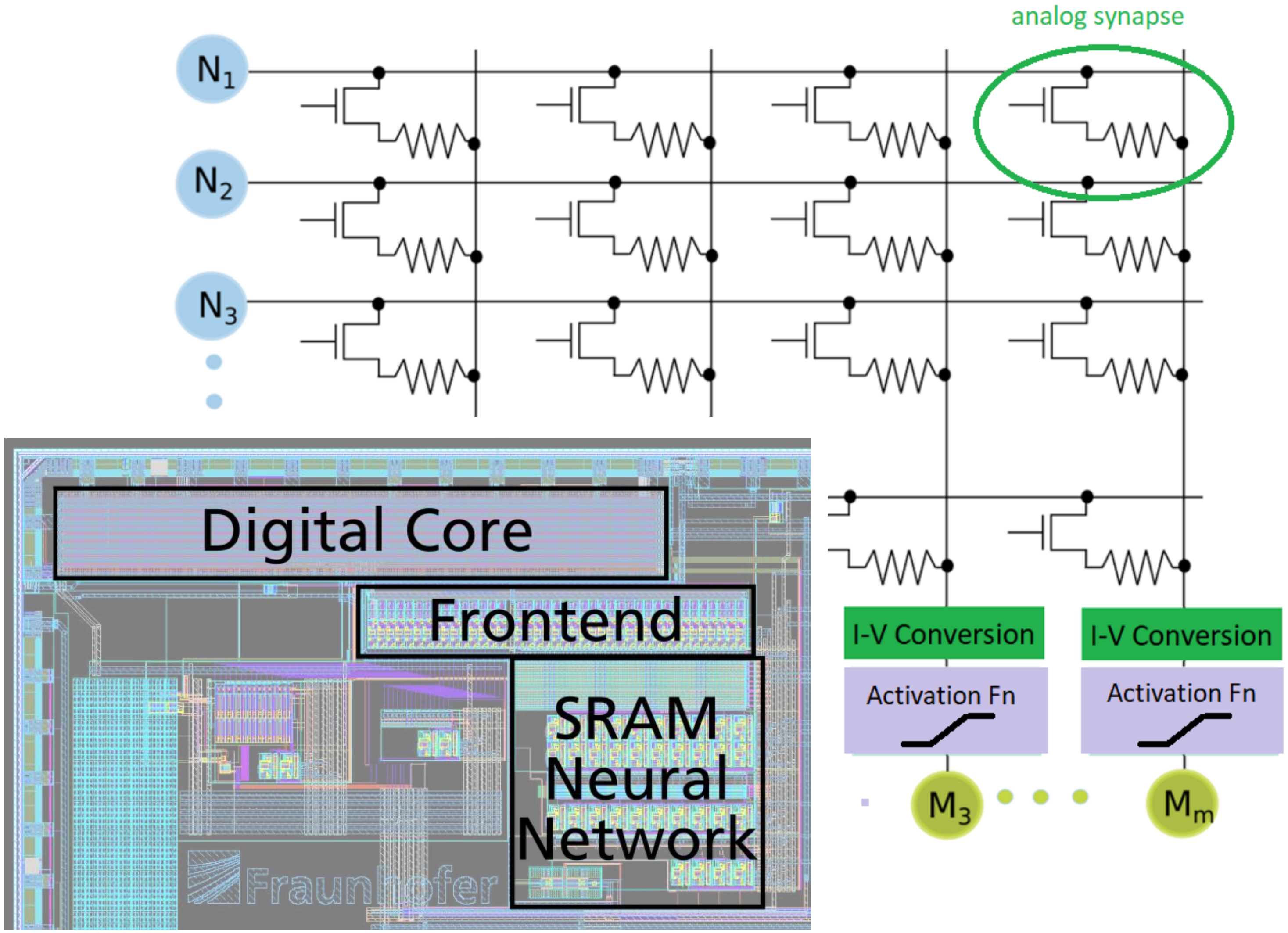
Presentation Outline

- Introduction
- Design and Implementation
  - DNN Top-Level
  - Synapse Circuit
  - Neuron Circuit
- Simulation Results
- Discussions and Conclusions

Introduction

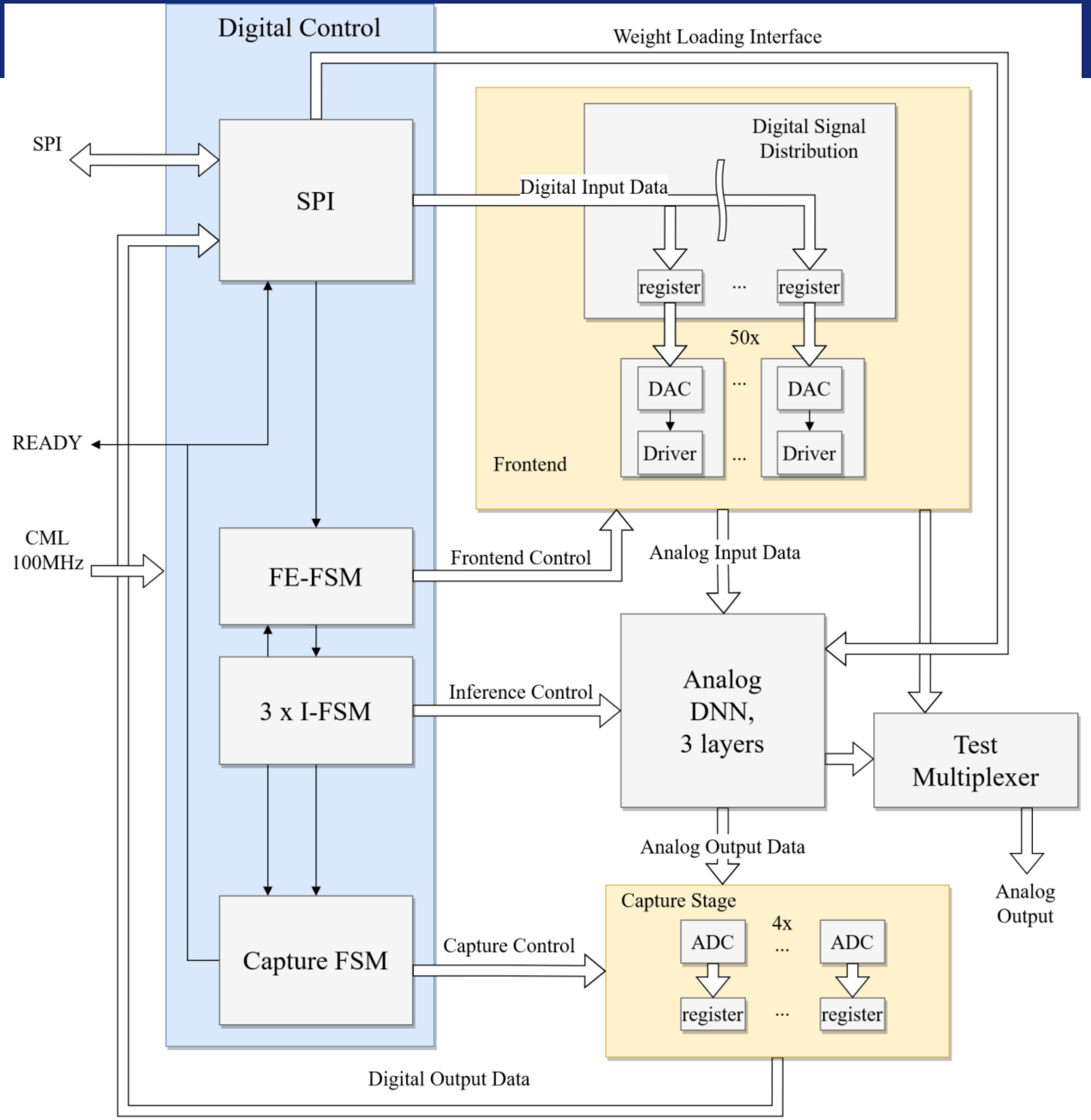
- Bring neural networks to edge devices requires
  - High energy efficiency
  - Low area

- Analog DNN accelerator a promising option but
  - Accurate calculations and
  - Robustness against PVT variations are challenging



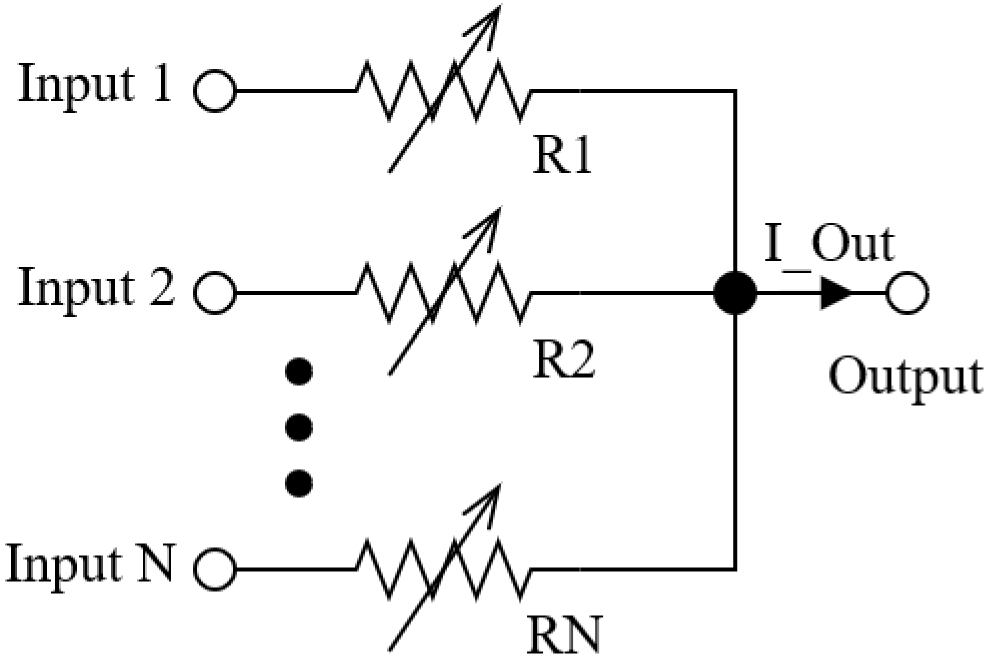
DNN Top-Level

- Digital control
  - Communication via SPI
  - DNN timing with FSMs
- Frontend
  - Digital-to-analog conversion
  - Driver stage for resistive DNN load
- 3-layer DNN
  - SRAM based synaptic weight storage
  - Fully connected
  - 50x20, 20x10, 10x4
- Capture stage
  - Analog-to-digital conversion



Synapse Circuit: State-of-the-Art

- Variable resistors to implement the weights
- V-I conversion
- Output node must be constant (virtual ground)
  - Transimpedance amplifier
  - Shunt resistor



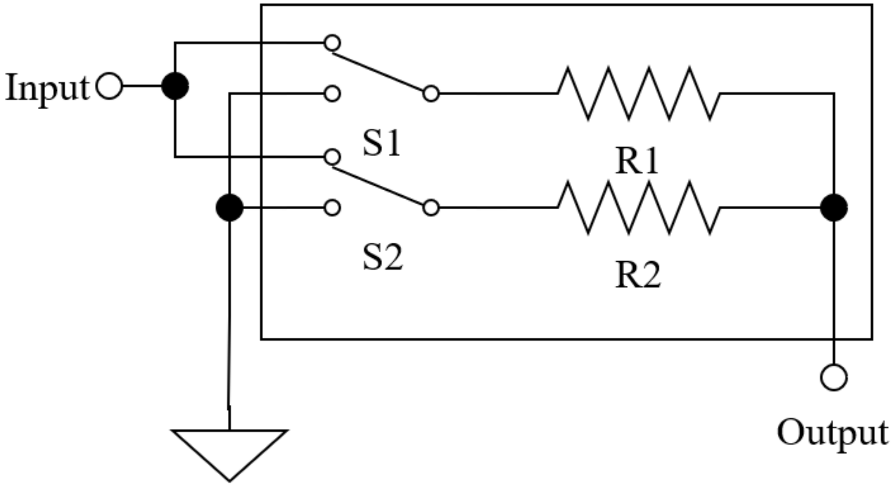
Synapse Circuit: Voltage Divider Approach

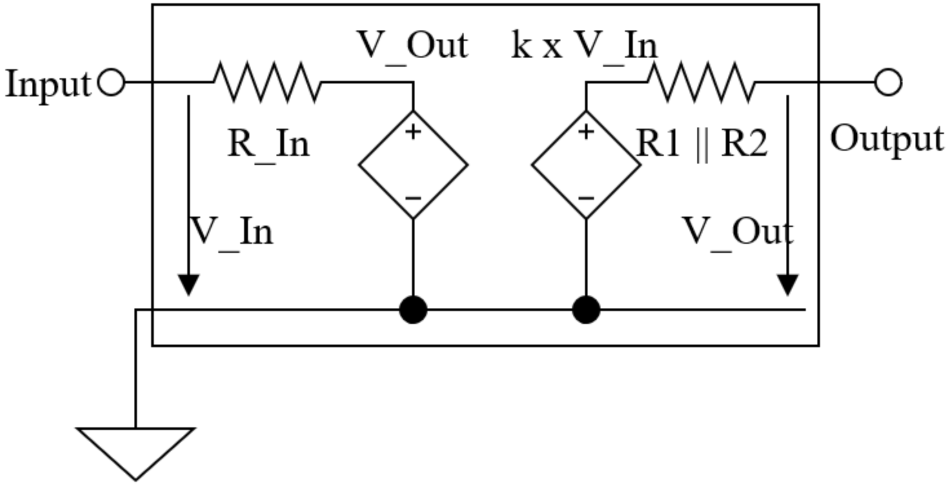
- Constant output resistance
- No virtual ground required

$$V_{OUT} = \frac{1}{N}\sum_{i=1}^{N} V_{In,i} \cdot k_i$$

→ Average operation

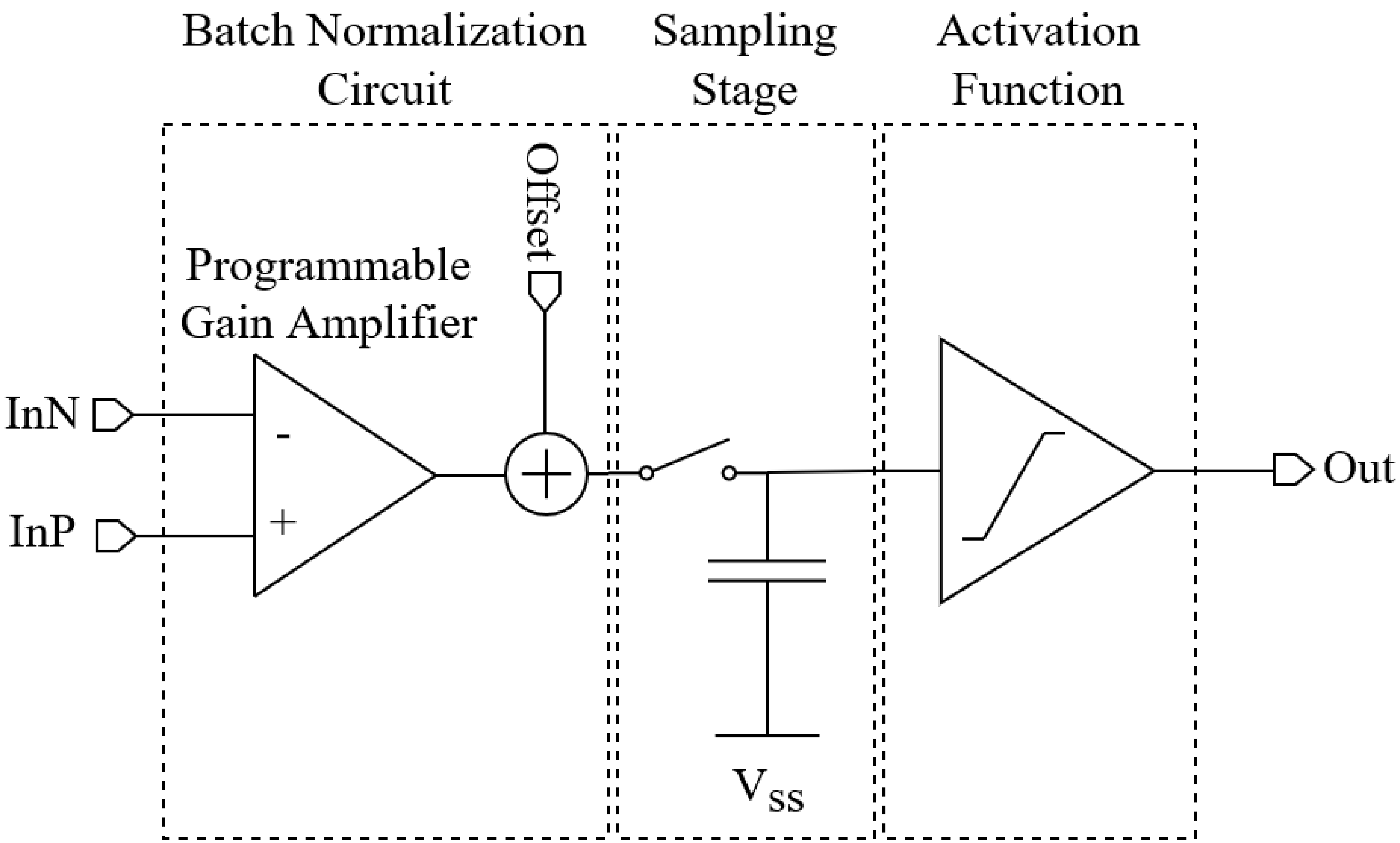
→ Gain required





Neuron Circuit

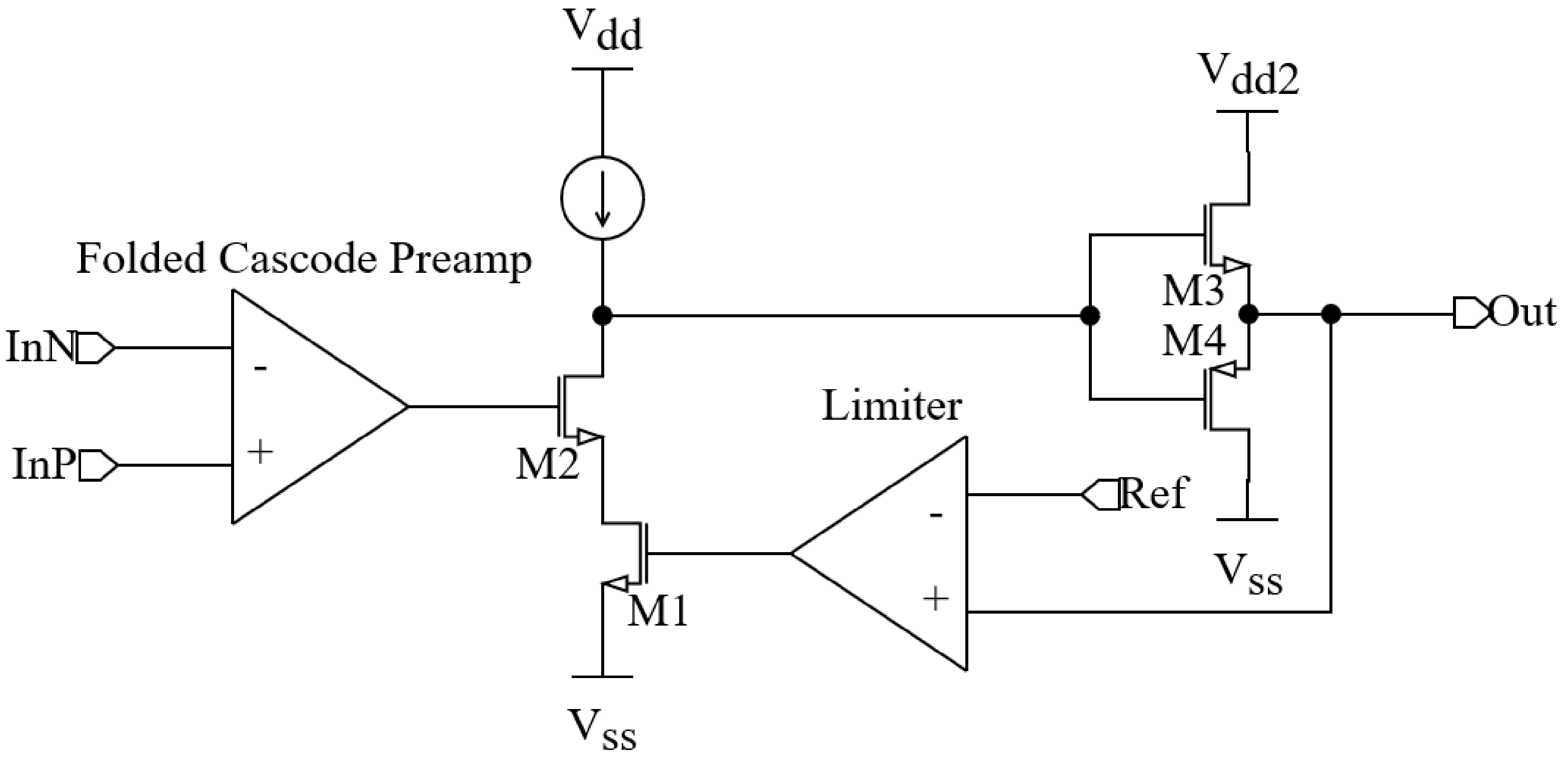
- Batch normalization circuit
  - Programmable gain
  - Offset addition
- Sampling stage
- Non-linear activation function



Neuron Circuit – Activation Function

- Rectified Linear Unit
- Operational Amplifier

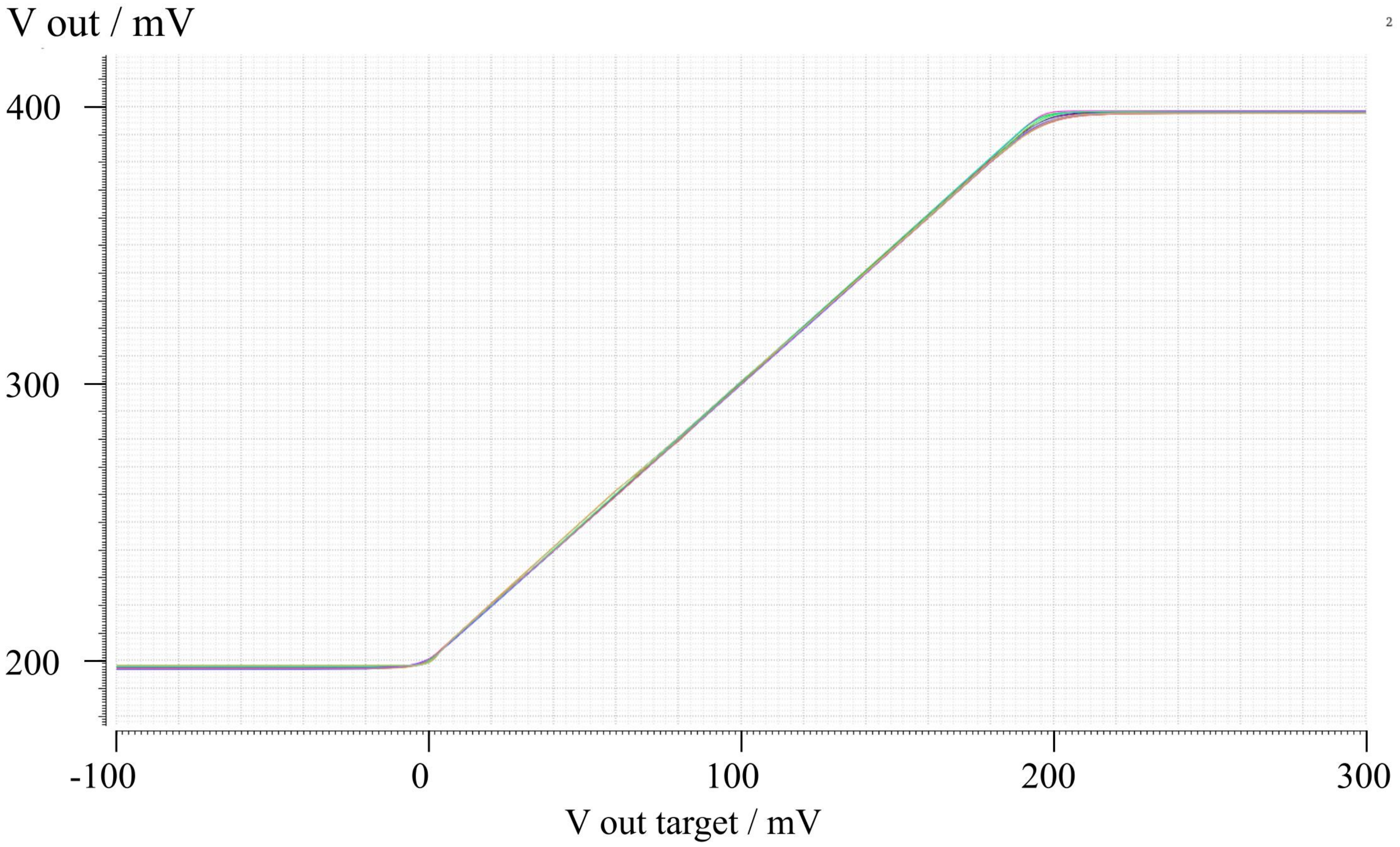
- Output range limited
  - Upper limit: Supply Voltage
  - Lower limit: Limiter



Simulation Results

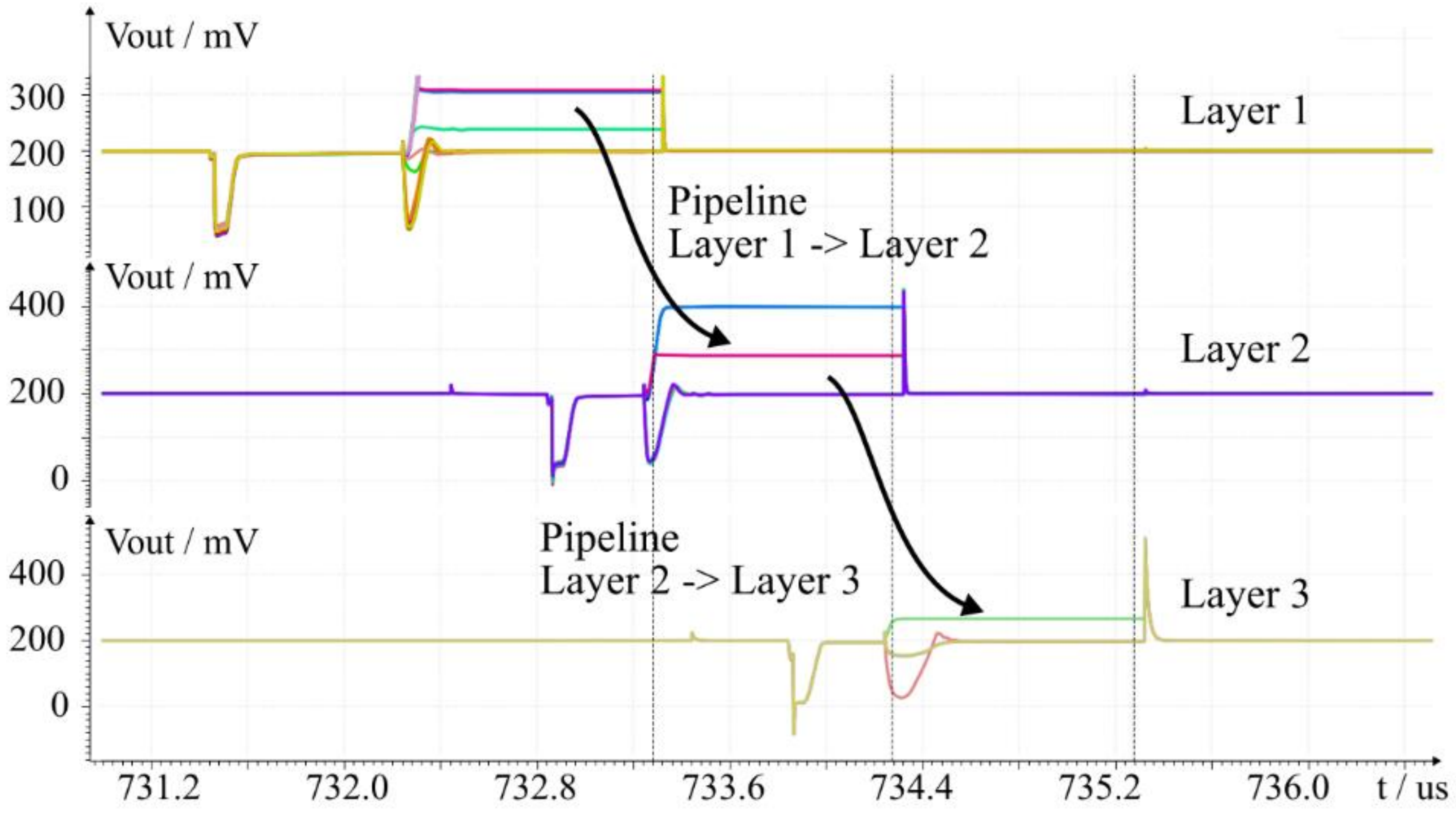
- Output range
  - Lower limit: 200 mV
  - Upper limit: 400 mV

- Minor deviations due PVT variations



Simulation Results

Parameter	Value
Average Deviation	1.9 mV
Maximum Deviation	6.9 mV
Energy/ Inference	9 nJ
Latency	5 µs
Power Efficiency	276 GOPS/W



Discussions and Conclusions

- Accurate DNN computations even with PVT variations due to synaptic circuit based on a voltage divider approach and robust neuron circuit
- Proof-of-concept simulation results show
  - Functionality of the in-memory computation approach
  - Low energy consumption
  - Low latency
- Test strategy with test patterns for functional verification, evaluation and KPI measurement has been developed
- Evaluation and verification through measurement still pending

Event Organisers

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Thank You

For your attention

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