The International Workshop on Edge Artificial Intelligence for Industrial Applications (EAI4IA)

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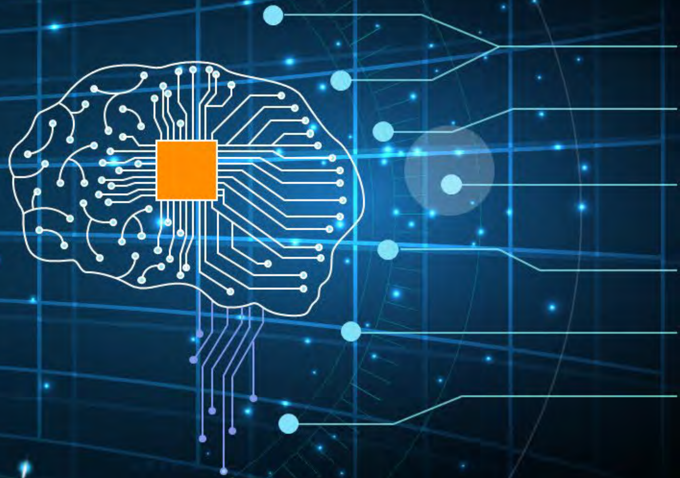

Vienna, Austria

25-26 July 2022

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AI machine vision system for wafer defect detection

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Vienna, Austria 25-26 July 2022

VTT Micronova research centre

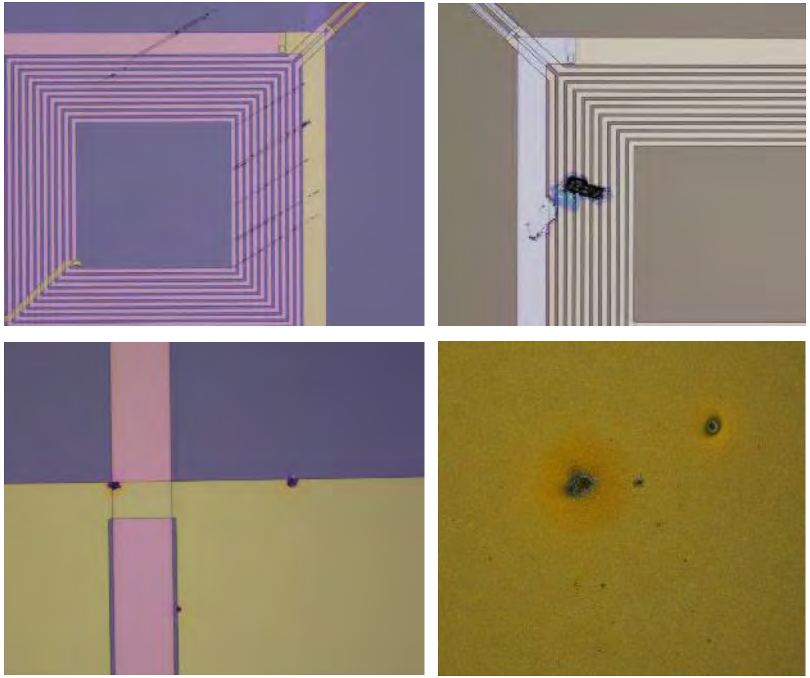
VTT

- Finland's national research infrastructure for micro-, nano- and quantum technology
- Largest R&D cleanroom facility in Northern Europe
- Offers cleanroom services and the entire development cycle of micro- and nanofabrication

Cleanroom defect inspection

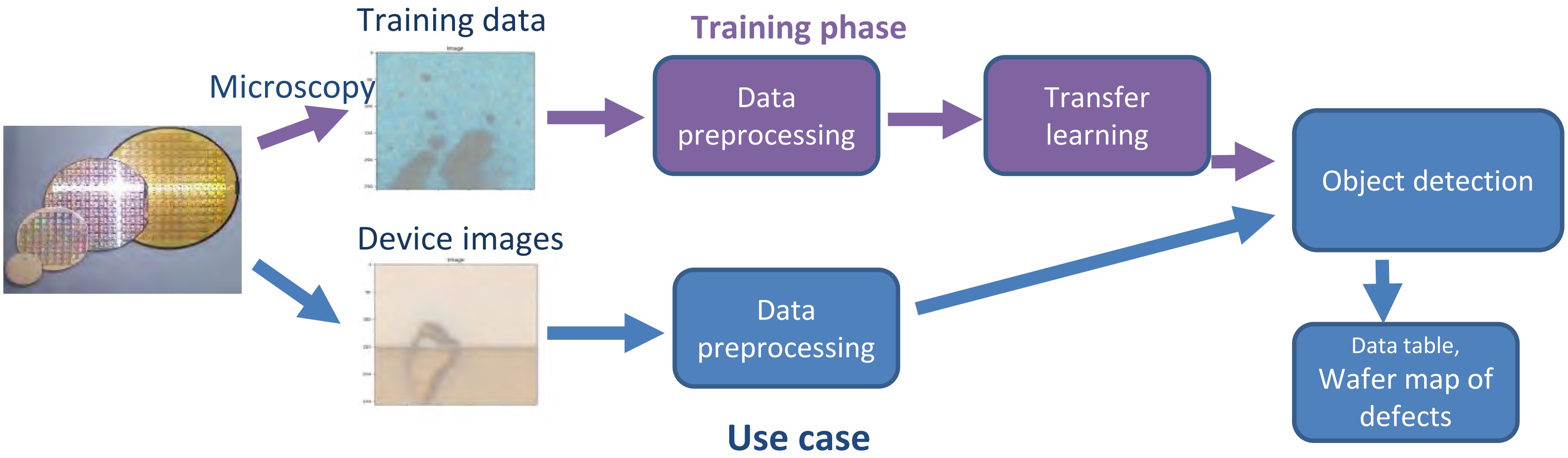
- Hundreds of wafers are processed every day at the Micronova cleanroom
- Defects are unavoidably generated at different steps of wafer processing
- Currently the defects are detected manually, which is time-consuming and tedious
- Wafer inspection and defect detection process should be automated
- Approach: Object detection neural network integrated with an optical scanning microscopy system
- The system is developed under the ECSEL AI4DI project

Microscopic images:

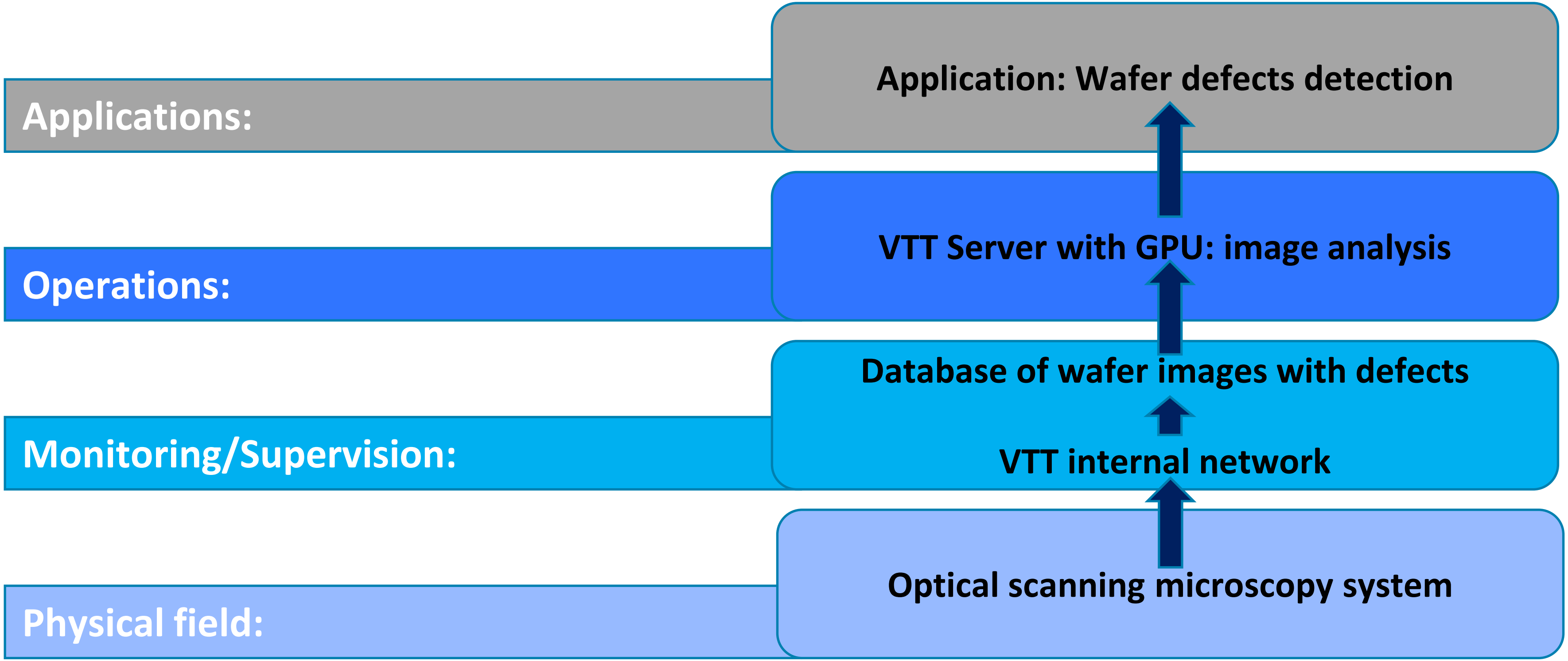


System description

- Semiconductor or superconductor device wafers are scanned using an optical scanning microscopy system
- Machine learning algorithm is used to detect silicon wafer defects
- The detection results are provided in a readable form either as a data table or as a defect heatmap



AI Architecture



Hardware layer and AI frameworks

VTT

HW: PC/server with NVIDIA Quadro RTX 5000 16GB GPU at the VTT Micronova cleanroom connected to the optical scanning microscopy system Muetec CD3000 through the internal network

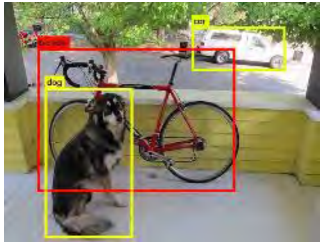
Image specifications:

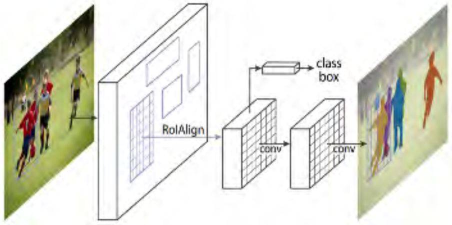
- **5x magnification**
- **png format (or bmp converted to png)**
- **1600x1200 px resolution**

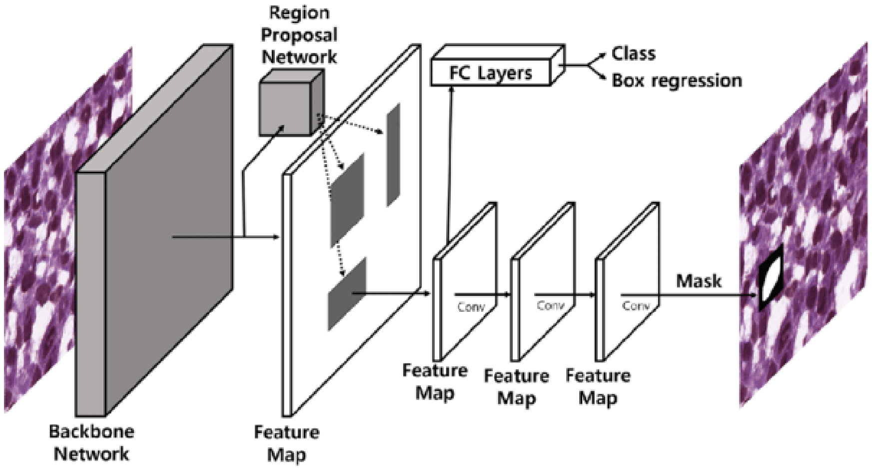
SW: Python Tensorflow, Python, Nvidia CUDA

AI for defect detection

- Object detection models (Mask R-CNN, YOLO) can be used
- We are using state-of-the-art Mask R-CNN architecture on Python Tensorflow
- Mask R-CNN consists of two stages: first a Region Proposal Network proposes candidate object bounding boxes and the second stage extracts features using Region of Interest Pool from each candidate box, then performs classification and bounding-box regression and outputs a binary mask for each Region
- The ResNet-101 convolutional backbone architecture was used for feature extraction over an entire image







AI methods

Data Pre-processing:

- Collection of wafer images with various defects at different processing steps
- Data augmentation by mirror and rotation transformation to reduce overfitting
- The dataset was split into training and validation sets, containing 935 and 165 images each

Modelling

- Mask R-CNN algorithm implementation
- Transfer learning using Common Objects in Context (COCO) dataset
- Iterative optimization of the detection accuracy by optimization of the training dataset

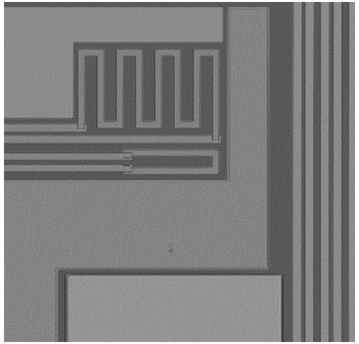
Microscopic images are preprocessed for AI training:

Original image — Defect labelling and image crop — Data augmentation

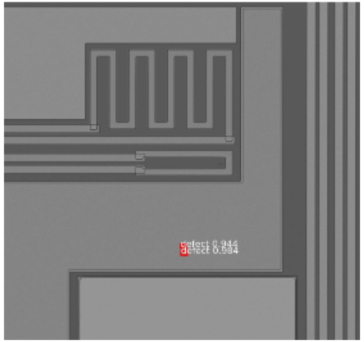
Achievements

- The AI algorithm passed several rounds of optimization and testing using microscopic images of various semiconductor and superconductor devices
- Graphical user interface was implemented
- The system provides binary classification: defect vs background with results available in both graphical and text formats
- Latest dataset of 192 images showed accuracy of 86% correct detections with detection time of 1-2 sec per image
- The AI software was installed on a separate server at VTT and is now connected with the optical microscopy scanning system through the internal network

Binary classification (defect vs background):



Test image



AI detection of defects

AI4DI Defect detection, summary table

	PUB	slot	chip	position	area	probability	x position	y position	image
1	24	14	1	1	99	0.8933772	188.5	1071.5	PUB24_slot14_chip1_pos1.png
2	24	14	1	1	72	0.8429125	766.5	1154.0	PUB24_slot14_chip1_pos1.png
3	24	14	1	2	182	0.9842441	1188.0	587.5	PUB24_slot14_chip1_pos2.png
4	24	14	1	2	156	0.943947	1186.5	572.0	PUB24_slot14_chip1_pos2.png
5	24	14	1	2	49	0.70072454	25.5	237.5	PUB24_slot14_chip1_pos2.png
6	24	14	1	3	208	0.98582953	1266.0	1003.5	PUB24_slot14_chip1_pos3.png
7	24	14	1	3	108	0.98534435	110.0	349.5	PUB24_slot14_chip1_pos3.png
8	24	14	1	3	100	0.9530289	1277.0	685.0	PUB24_slot14_chip1_pos3.png
9	24	14	1	4	110	0.9664215	1295.5	232.0	PUB24_slot14_chip1_pos4.png
10	24	14	1	4	56	0.81826836	1161.5	809.0	PUB24_slot14_chip1_pos4.png
11	24	14	1	5	783	0.99582374	906.5	389.5	PUB24_slot14_chip1_pos5.png

Discussion and Impact

Challenges:

- Preparation of a training dataset was very challenging. At VTT different teams work on very different devices. The dataset should have included lots of examples.
- Different defects look very differently (particles, scratches, photoresist, etc) and should all be detected.
- Only about 15% of the detected defects were critical for wafer processing. The criteria of a defect being critical or non-critical is very device-specific and cannot be easily generalized. After the system provides the detection results, the final decision on the importance of the defects for processing had to be made by the cleanroom experts.

Expected impact:

- The system provides wafer defect detection with accuracy comparable to a human expert
- The overall working time required for wafer defect inspection is reduced
- The system will help saving valuable working time of cleanroom experts, improve fabrication yield and reduce fabrication cost

Event Organisers

The Key Digital Technologies Joint Undertaking - the Public-Private Partnership for research, development and innovation – funds projects for assuring world-class expertise in these key enabling technologies, essential for Europe's competitive leadership in the era of the digital economy. KDT JU is the successor to the ECSEL JU programme. www.kdt-ju.europa.eu

ECSEL Joint Undertaking

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Thank You

For your attention

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