The International Workshop on Edge Artificial Intelligence for Industrial Applications (EAI4IA)

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Vienna, Austria

25-26 July 2022

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An End-to-End AI-based Automated Process for Semiconductor Device Parameter Extraction

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Matthias Ludwig
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infineon

COGNITION FACTORY

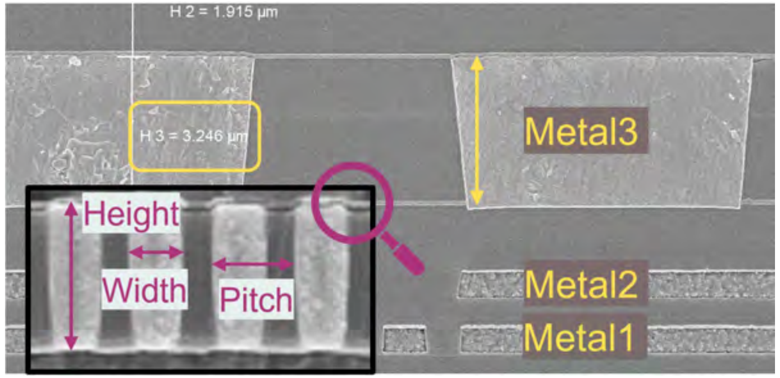
Vienna, Austria 25-26 July 2022

Presentation Outline

- Introduction and Background
- Task Overview
- Data Preparation Pipeline
- Semantic Segmentation
  - Architecture benchmark
  - Hyperparameters
- Parameter Extraction
- Synopsis and Overview

Introduction and Background

- Process automation for internal semiconductor device **analytics and counterfeit detection**
- **Counterfeiting activities** endanger safety, reliability and trust in critical systems
- Anti-counterfeiting methods: electrical testing, supply chain measures, design measures (PUF, logic locking, etc), **physical inspection**
- Relevant features for physical inspection:
  - Geometrical shapes and dimensions
  - Material-related properties



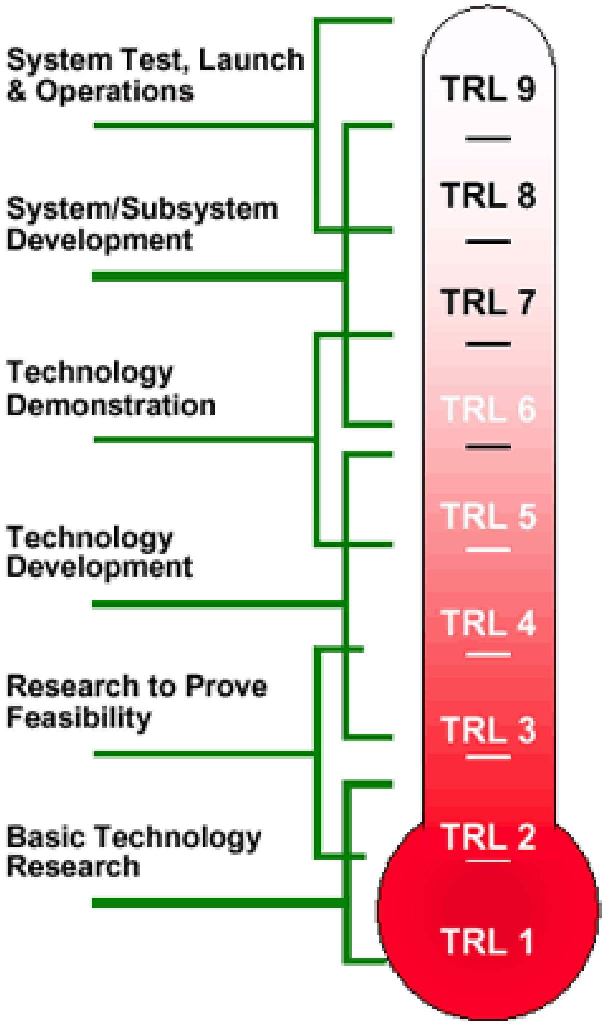
Counterfeit Electronic Parts:
A Multibillion-Dollar Black Market
by Brett Daniel, on Jul 27, 2020, 4:36:07 PM [1]

Counterfeit Chips on the Rise
A more firms report finding phony chips, the danger they pose becomes clearer
By Celia Gorman [2]

Combating Counterfeit Chips
How secure provisioning of cryptographic keys can fight the billions of dollars in counterfeit components.
AUGUST 6TH, 2020 – BY: PAUL KARAZUBA [3]

[1] trentonsystems.com/blog/counterfeit-electronic-parts
[2] spectrum.ieee.org/computing/hardware/counterfeit-chips-on-the-rise
[3] semiengineering.com/combating-counterfeit-chips/

Introduction and Background



- Workhorse in the field of automatization
- Constantly increasing rate of innovations
- Plethora of relatively low TRL methodologies with potential use-cases in industry

- AIM: Harness AI-based techniques and develop methodologies for subsequent quick and efficient use-case expansion

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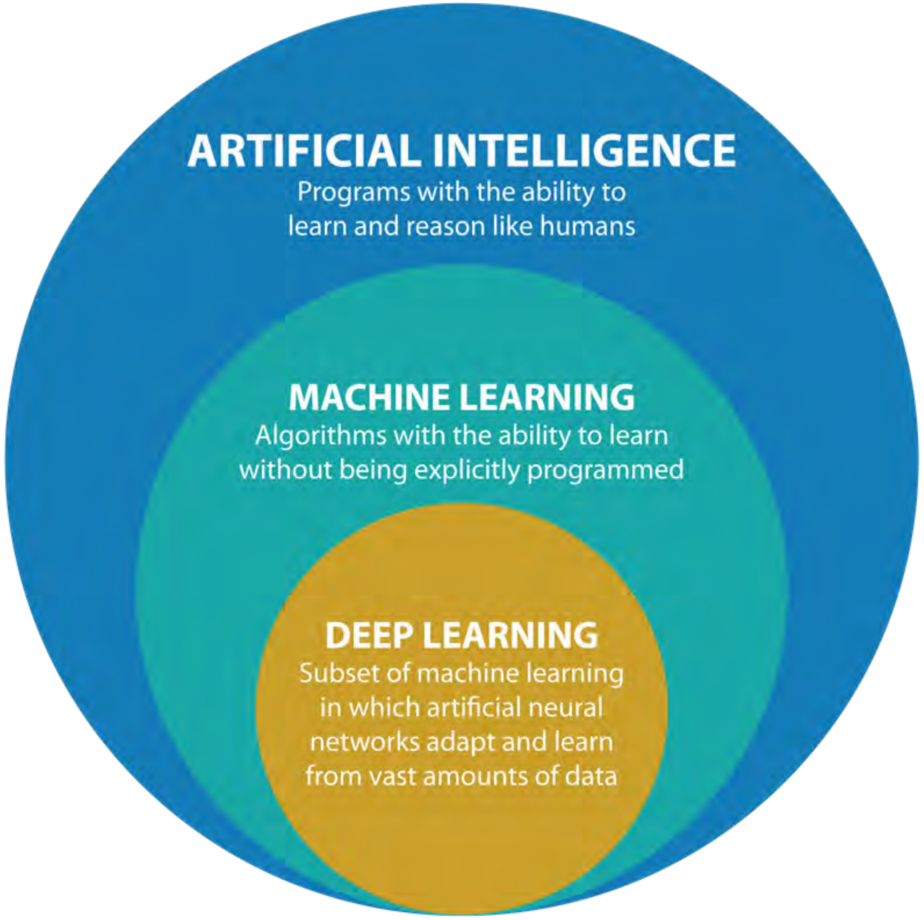
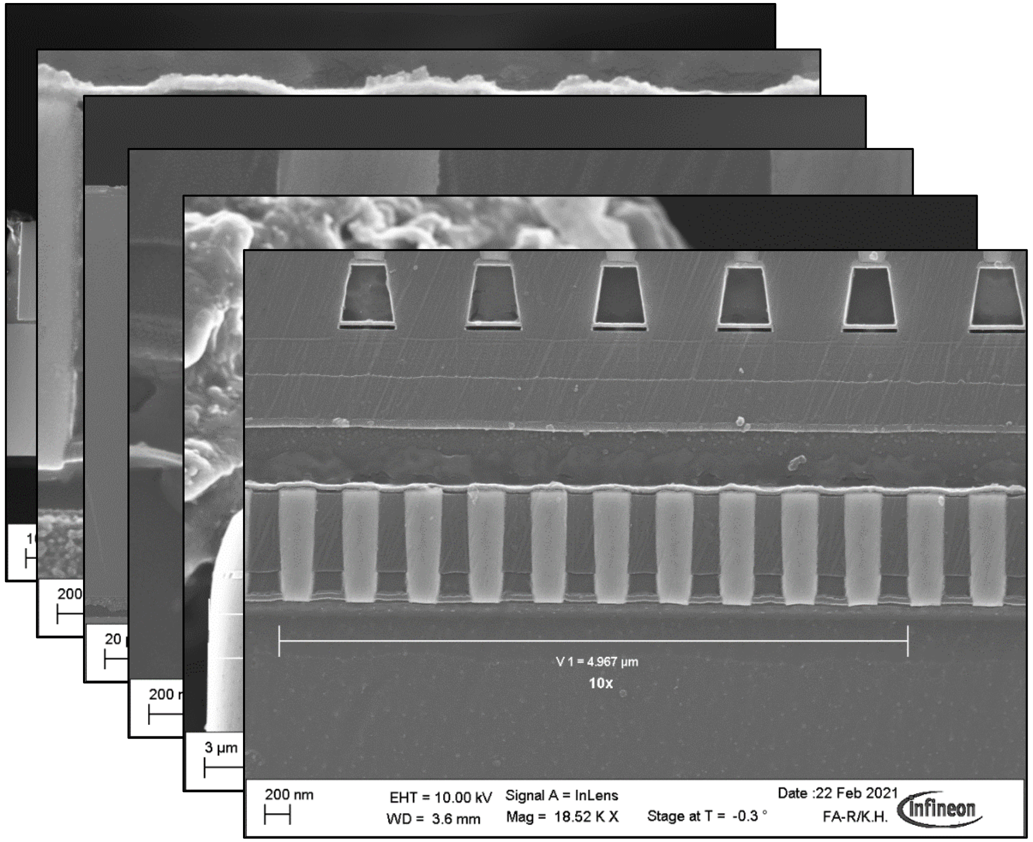


End-to-End Pipeline

- Task: Reverse Engineer the Technology



Product from:

ABC
Design House

Technology Definitions

⋮

Tech_A32_180
Tech_F53_90
Tech_D65_180_dti
Tech_V87_90
Tech_A21_180
Tech_V76_65
Tech_G09_250
Tech_C46a_180
Tech_C46b_90

⋮

Match

› **Automate** the process of transition from **raw SEM images** to **techonolgical fingerprint**

Application Overview

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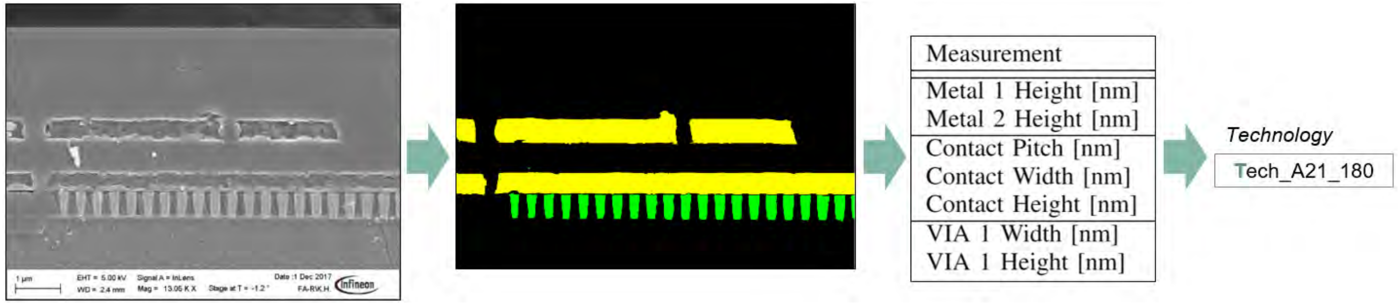
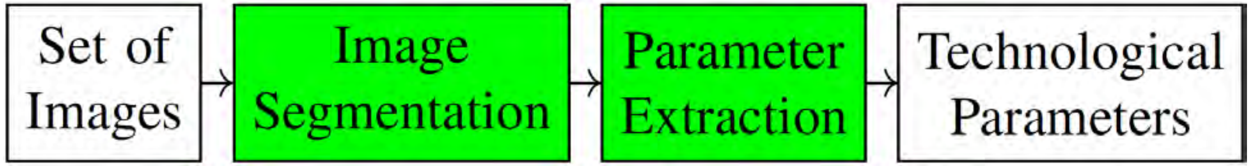
- Semantic Segmentation Stage
- Parameter Extraction Stage

- Technical Requirements:
    - Ability to measure cross section input images
    - Ability to categorize technologies (anti-counterfeiting use-case)
    - Ability to perform without user interaction
    - Ability to perform analysis within real-time





Data Acquisition

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Production

Analysis

Design phase | Fabrication phase | Market

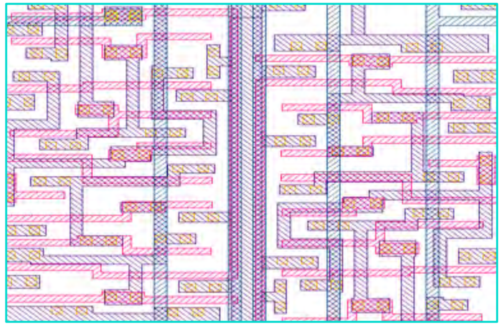
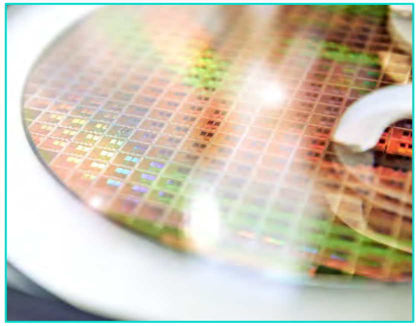
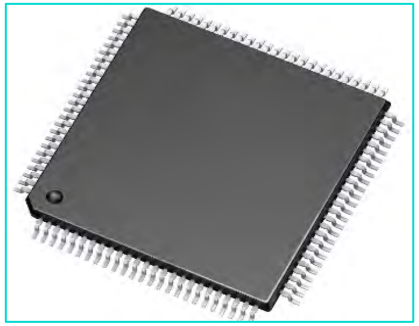
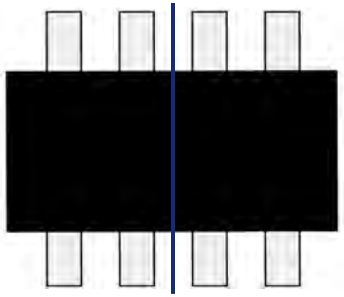

Layout

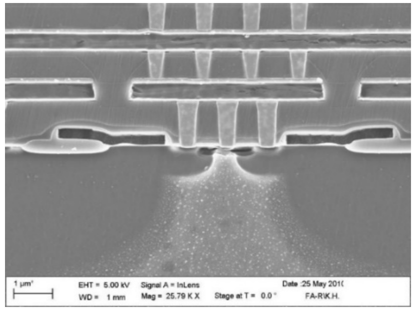

Photo masks


Wafer


Product


Product


Cross-Section (CS)

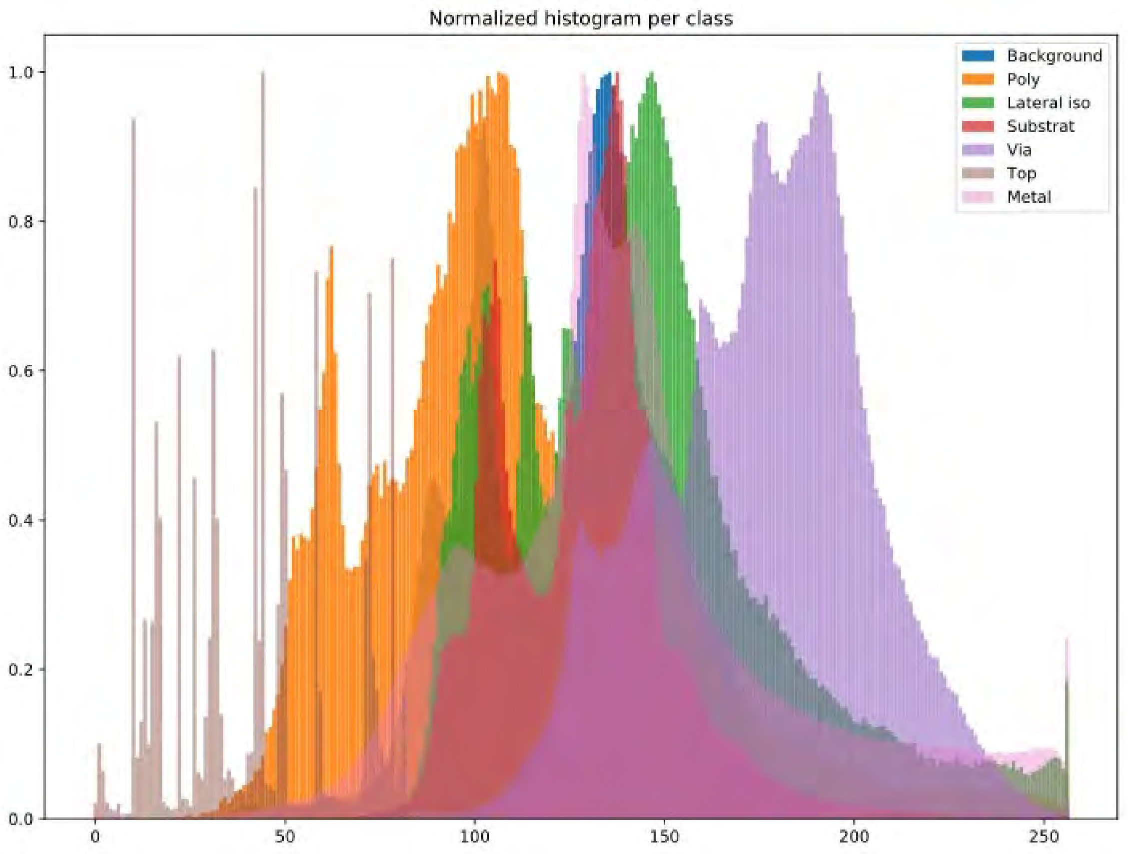

SEM Image of CS

Dataset and Labels

- Gray-scale images, acquired via SEM (1024 x 685) (Cu, Al-Tu technologies; 500nm – 40nm)

- Manually labelled:
  - **Metal**
  - **Vertical interconnect access (VIA)**
  - Poly
  - Lateral isolation/shallow trench isolation
  - Deep trench isolation

- Dataset size (60/20/20 split):
  - Benchmark stage: 202 images
  - Development stage: 2192 images



Dataset characteristics

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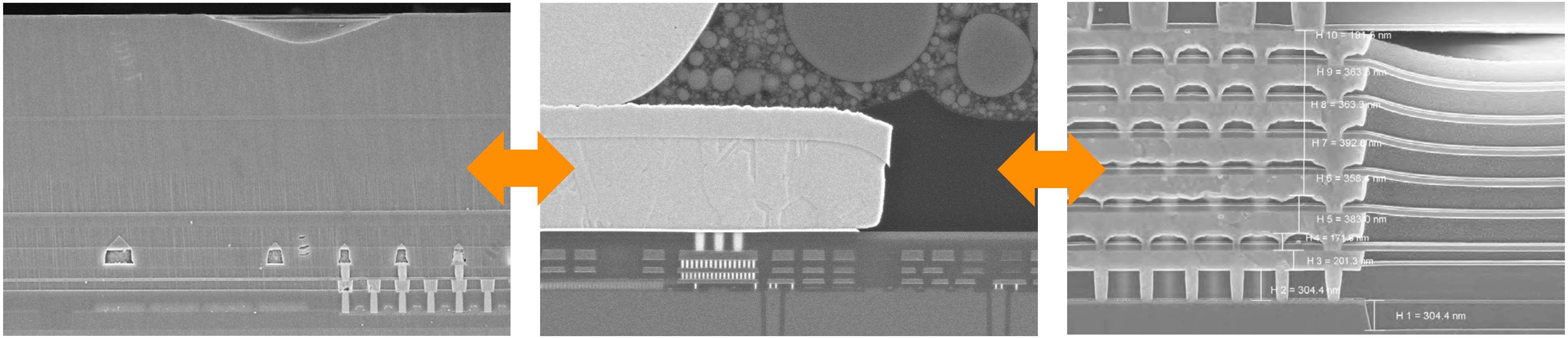
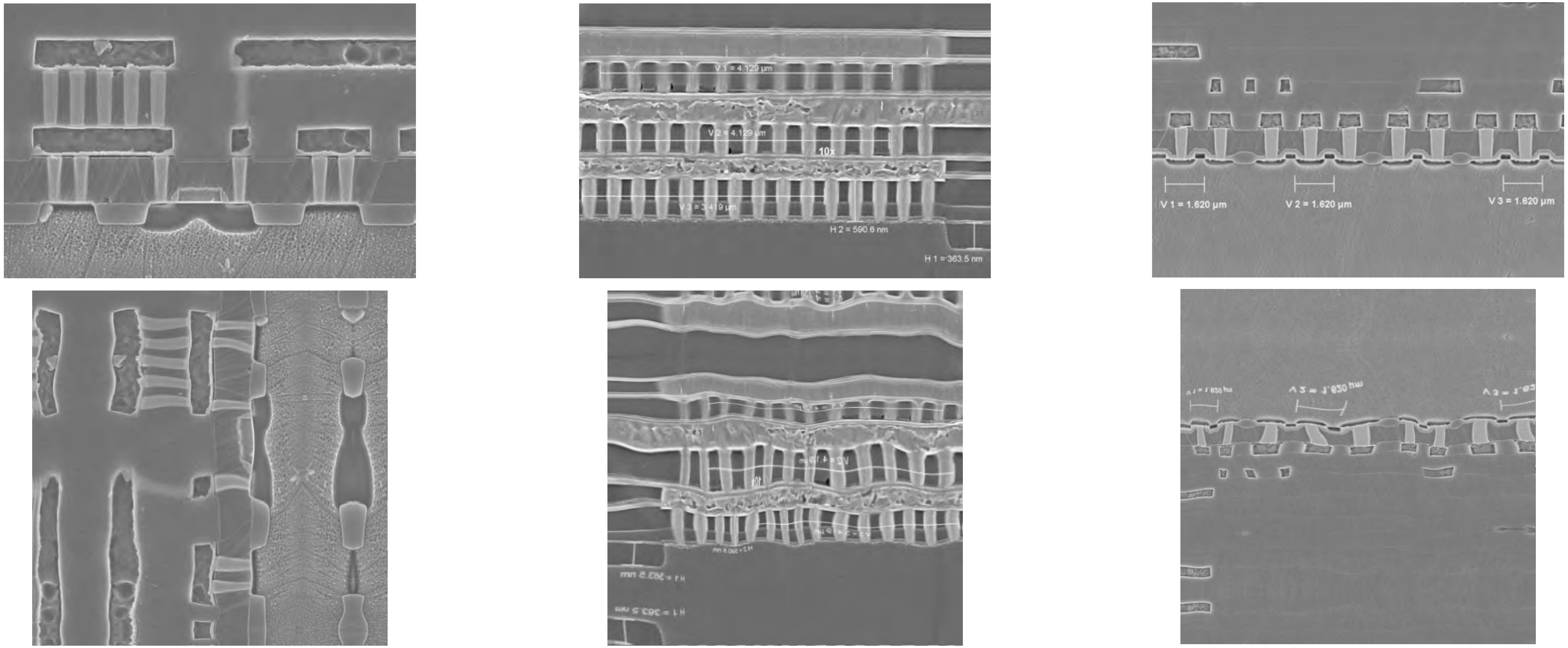
- Strong dependence on domain knowledge
- High input variances (both inter- and intra-image)
- Very high class imbalance



Data Augmentation

- Augmentation Procedures:
  - x90 Rotation, inversion, reflective padding
  - Elastic transforms
  - Grid distortion

Accuracy improvements >15%

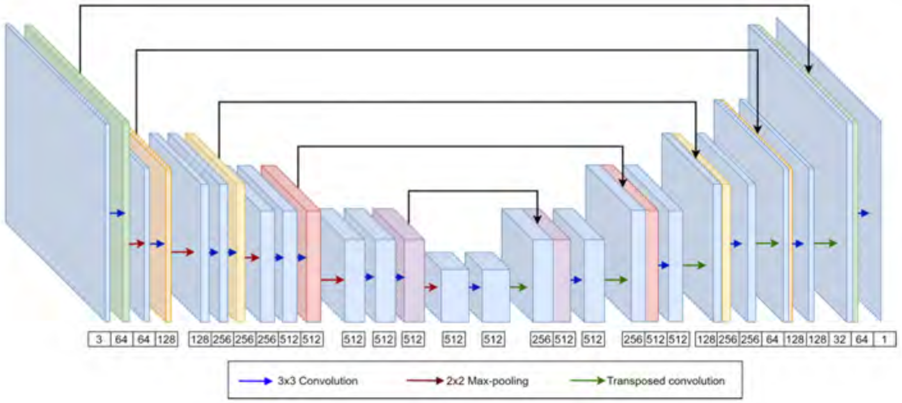


Original

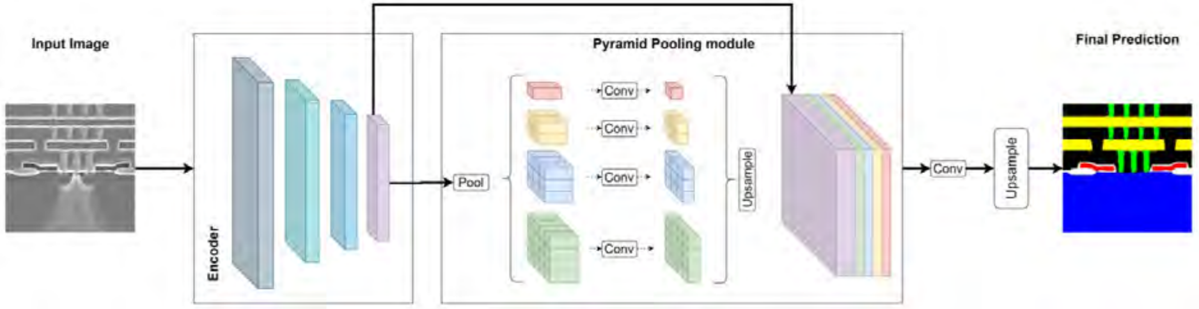
Augmented

Benchmark Candidates

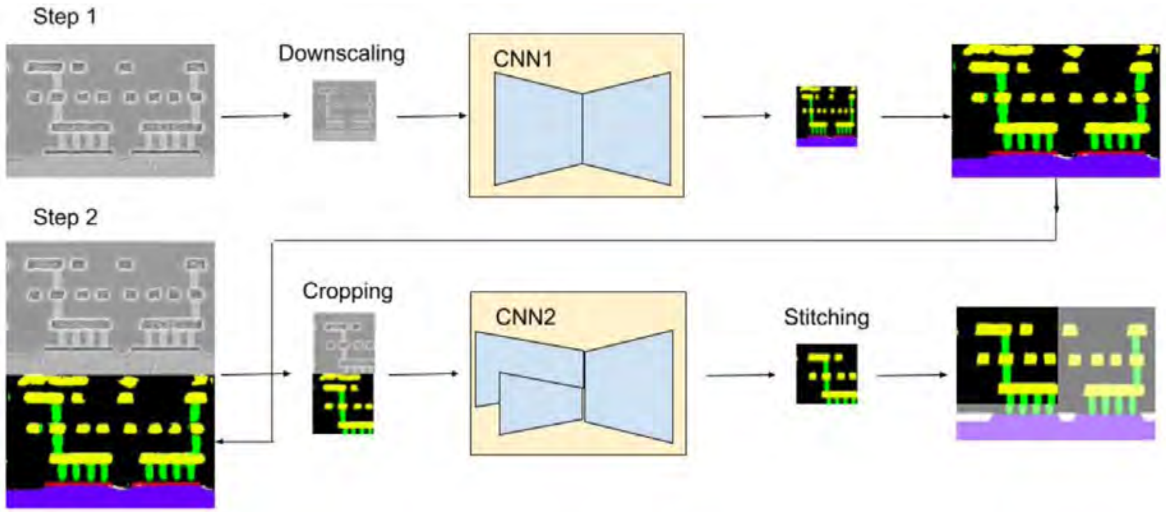
U-Net



Pyramid Scene Parsing Network (PSPNet)

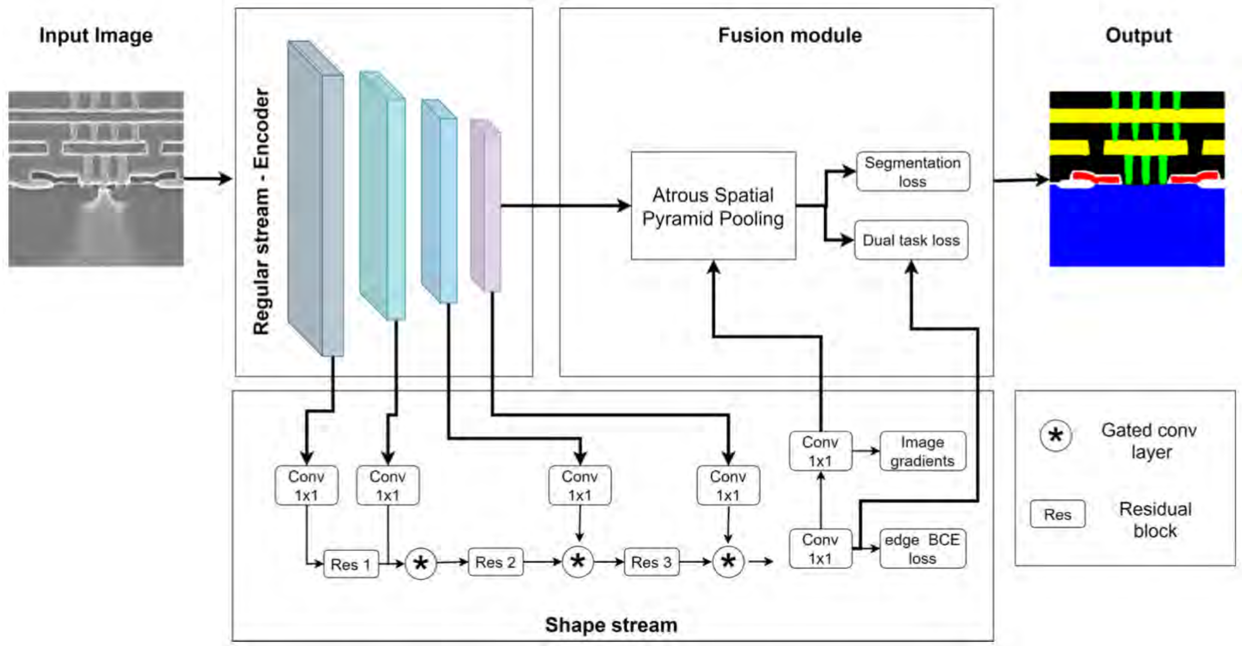


Siamese Network

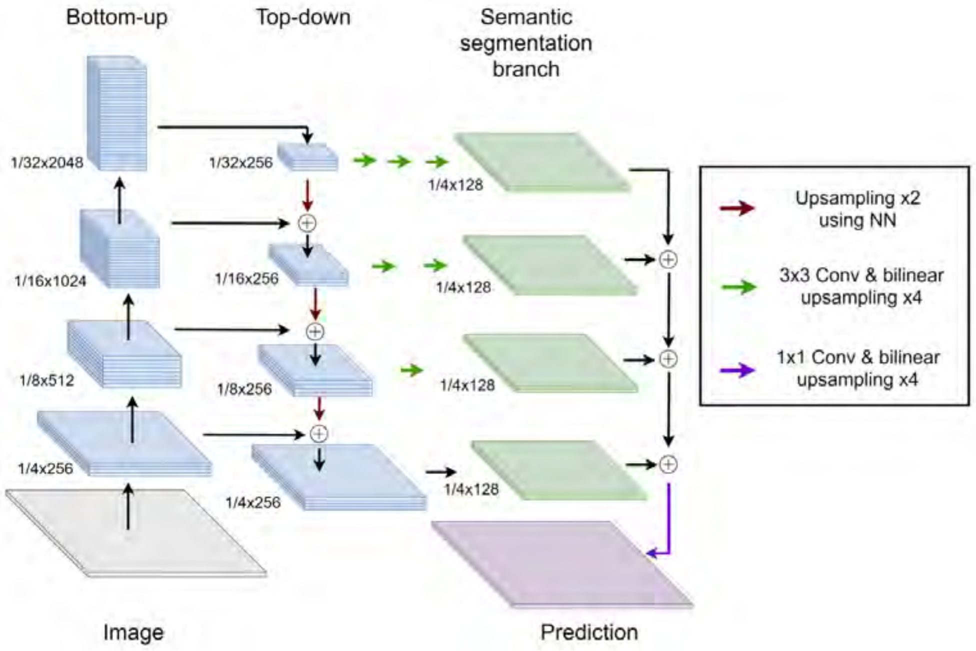


Benchmark Candidates

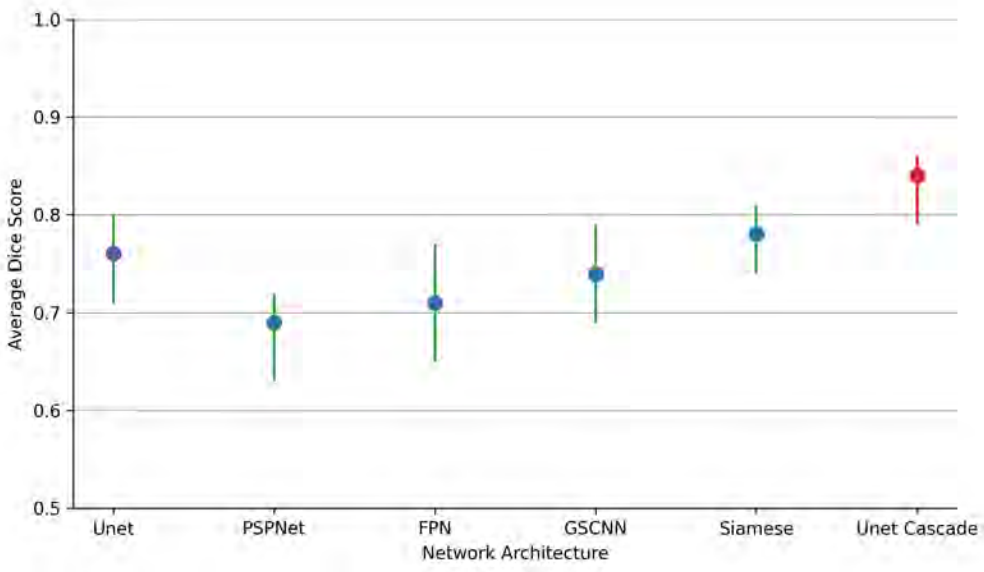
Gate-Shape Convolutional Neural Network (GSCNN)



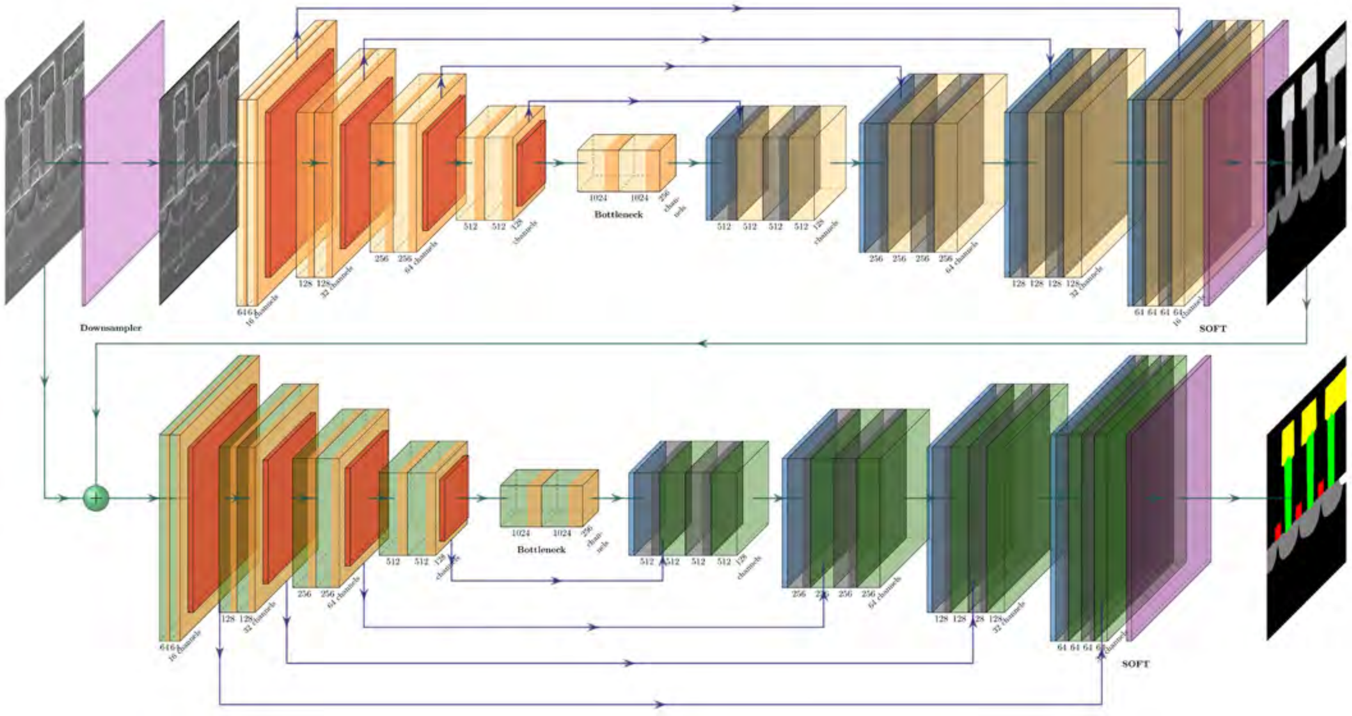
Feature Pyramid Network (FPN)



Benchmark Results



- UNet and Siamese networks most promising
- Cascaded UNet architecture
  - UNet generalisation capabilities
  - 2-step analysis inspired by Siamese architecture



Cascaded architecture of 2D and 3D UNets

Hyperparameters

- **Focal Tversky Loss** [metal]

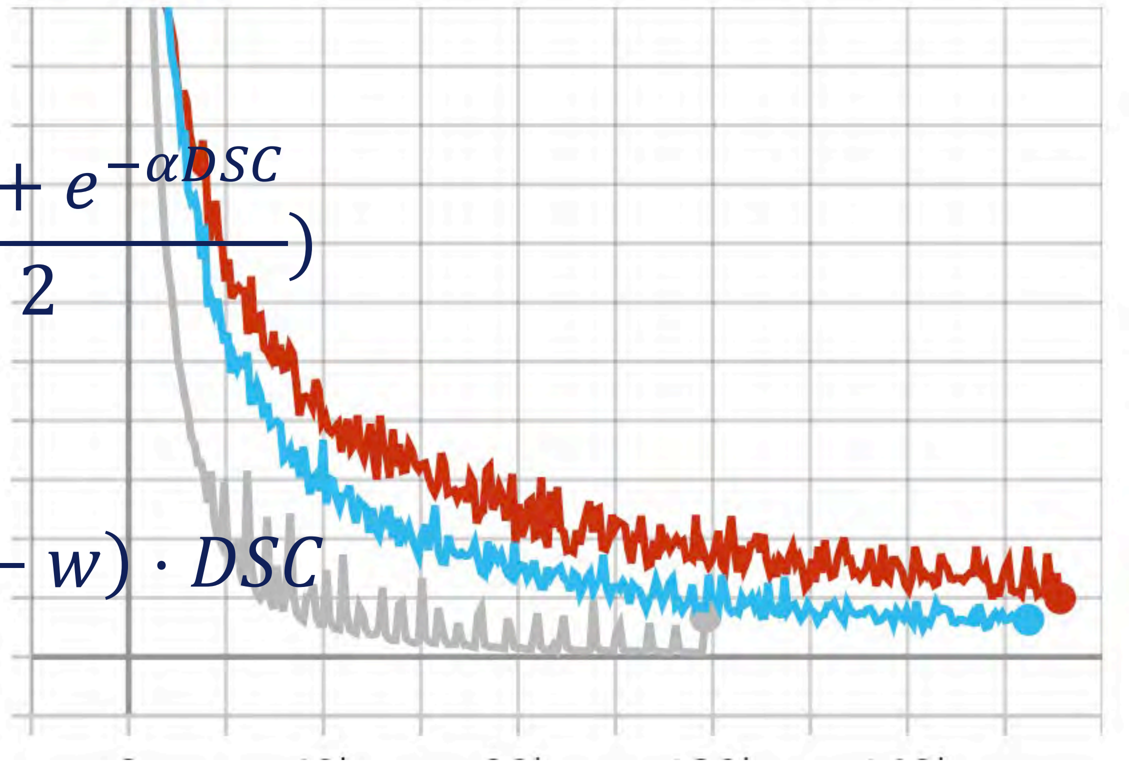
$$FTL = (1 - TI)^{\gamma}, TI = \frac{TP}{TP+\alpha FN+\beta FP}$$

- **LogCosh Loss** [VIA, Poly]

$$LCh = \frac{1}{\alpha}\log\left(\frac{e^{\alpha DSC} + e^{-\alpha DSC}}{2}\right)$$

- **Combo Loss** [Lateral ISO, Deep Trench ISO]

$$CoL = w \cdot CE - (1 - w) \cdot DSC$$



Hyperparameters

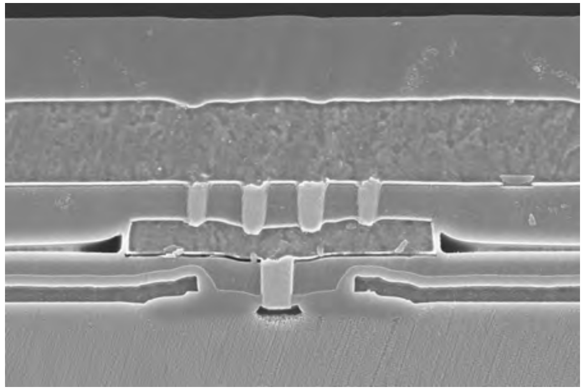
More complex Loss functions:

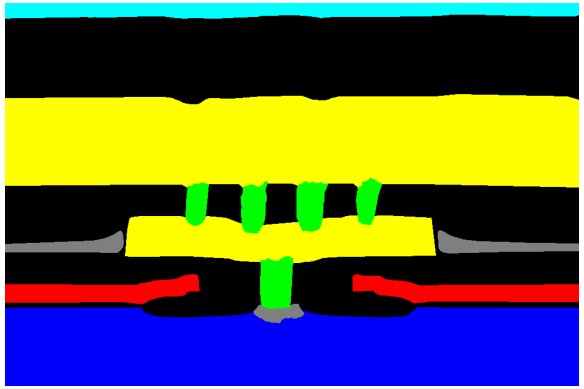
+Accuracy increase ≈15-20%

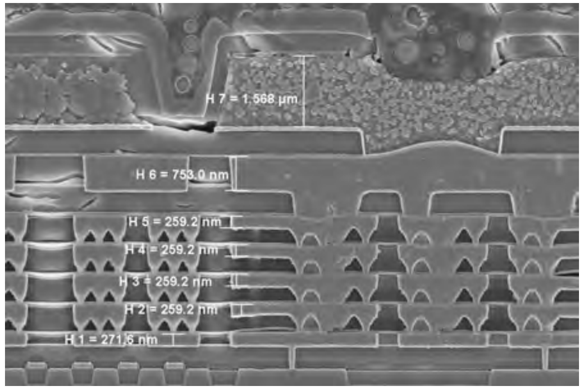
– More training time

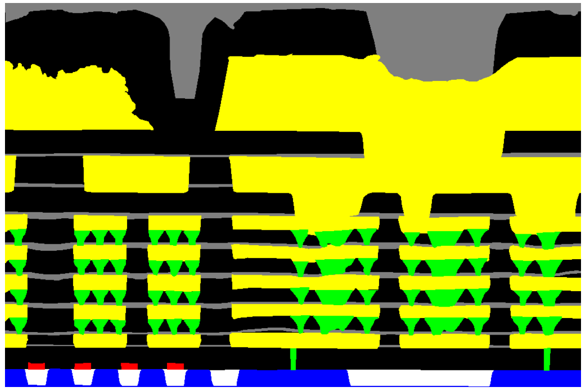
– More tune-able hyperparameters

– Higher GPU requirements (batch sizes 4 times smaller)





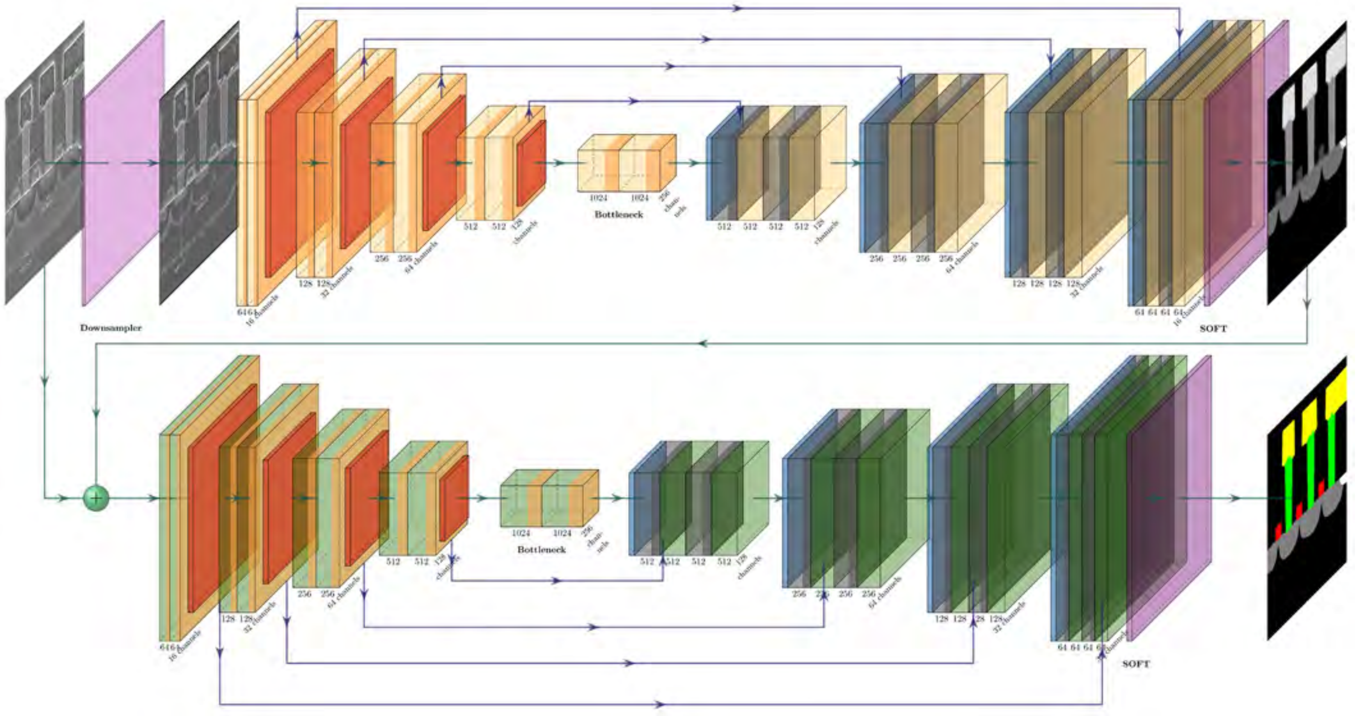




Benchmark Results

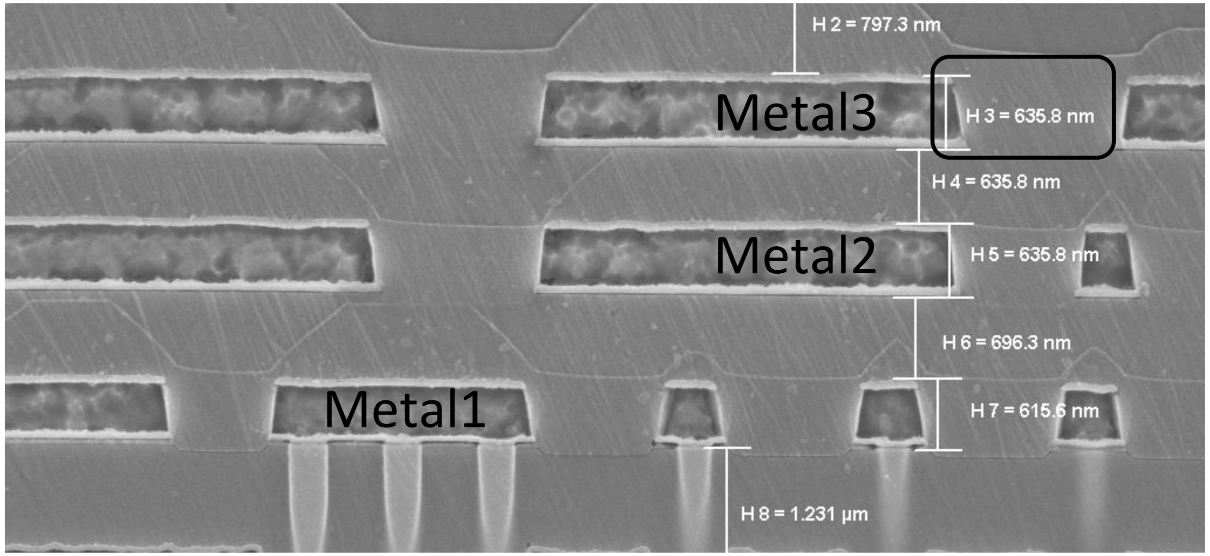
Label of Interest	Validation Dice Score
Metal	0.93
VIA	0.91
Poly	0.88
Lateral ISO	0.82
Deep Trench ISO	0.76

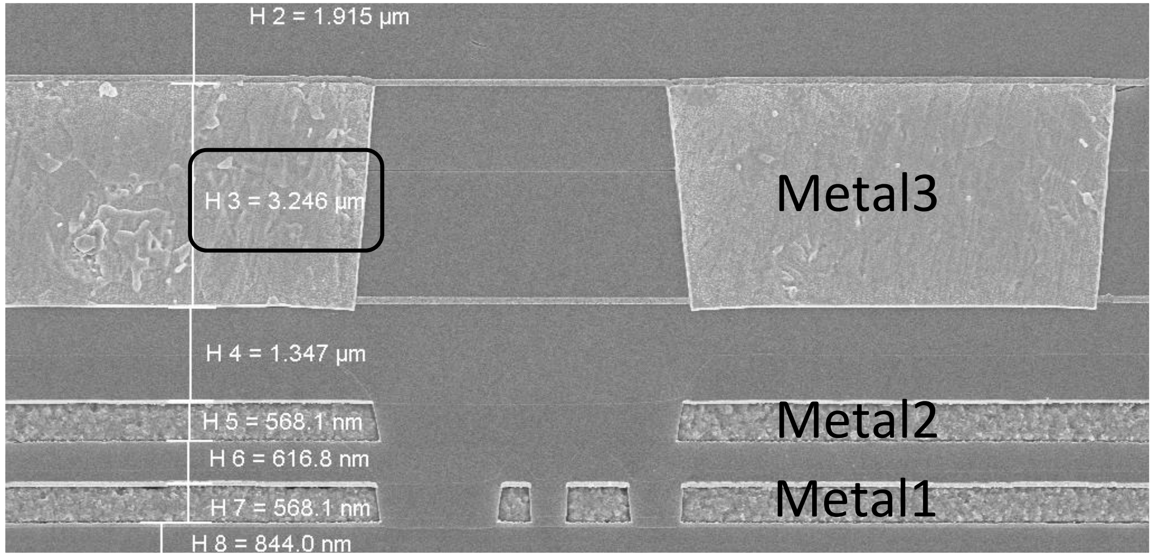
Final Validation Scores



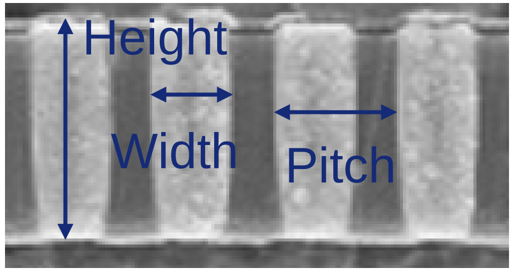
Cascaded architecture of 2D and 3D UNets

Differentiating Technologies

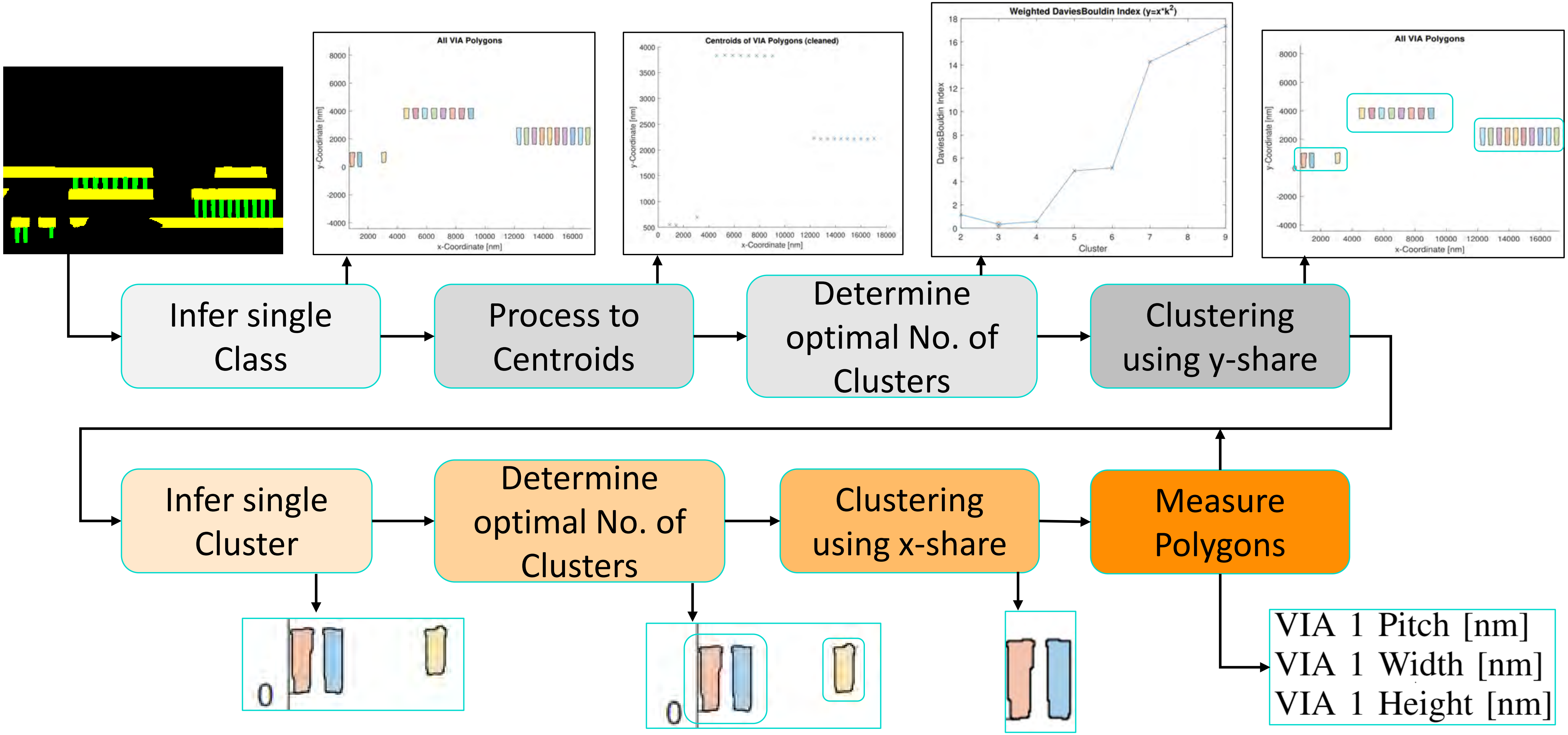




- In general, all features that allow an **inference of differences** between images (geometrical features, material-related features, even tool finger-printing)
- In the presented process, geometrical features (e.g. pitch, height, width) are measured



Interpretation of Results



Sample: Overview

- **Overall:** 53 image taken on 3 locations of CS
- Extremely large variance in pixel size (~factor 2000)

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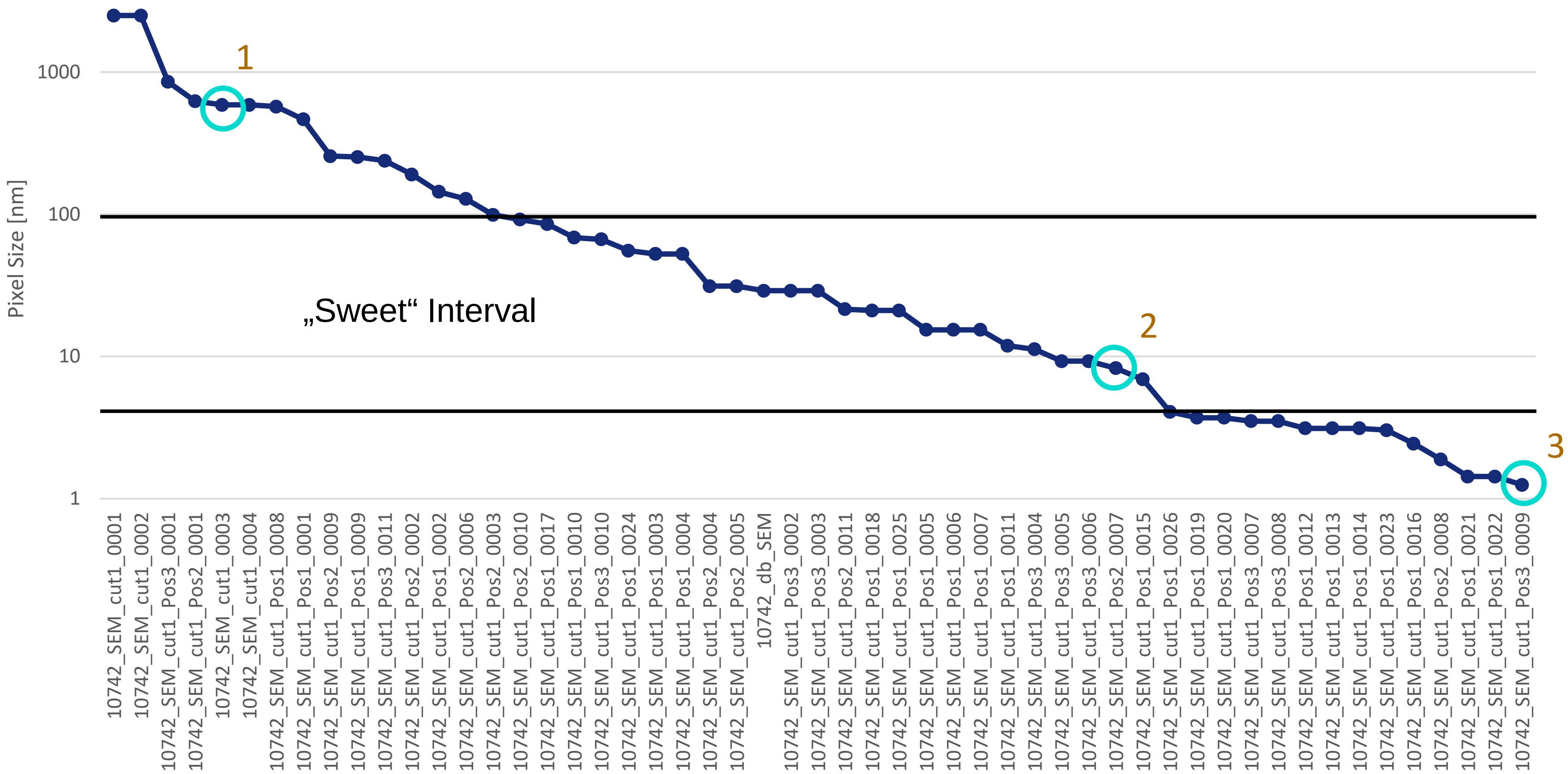
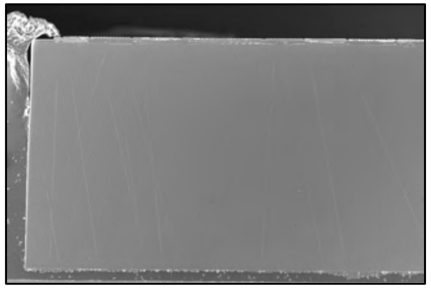


1



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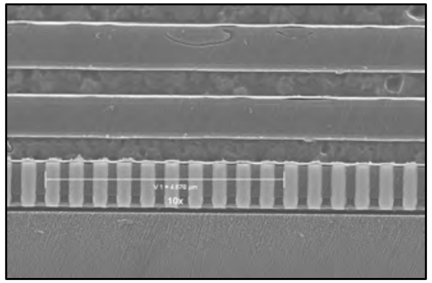

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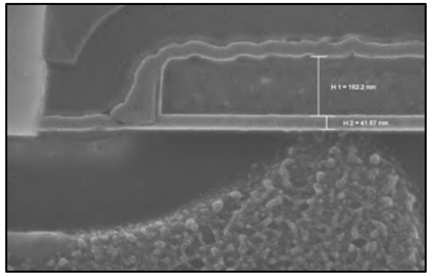
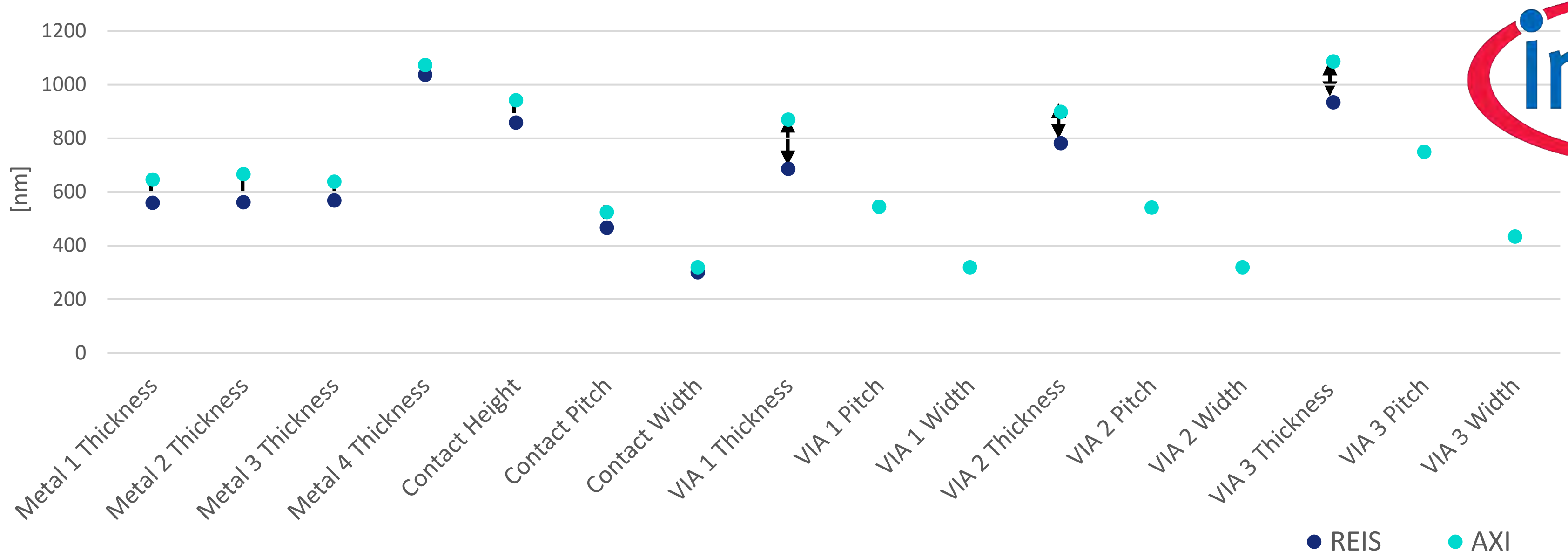
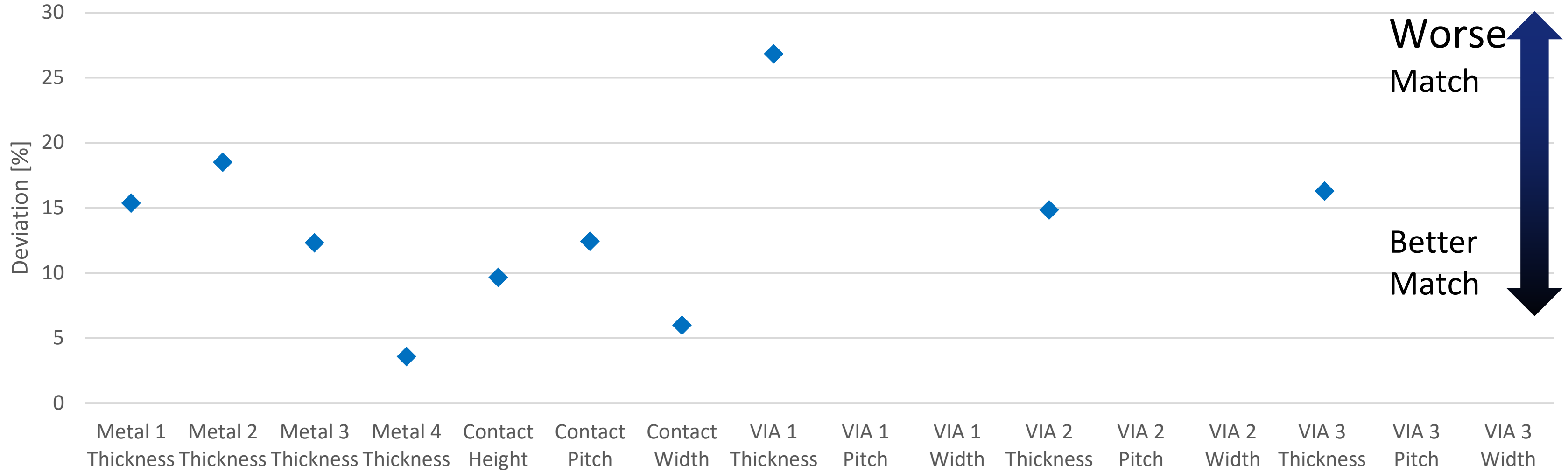
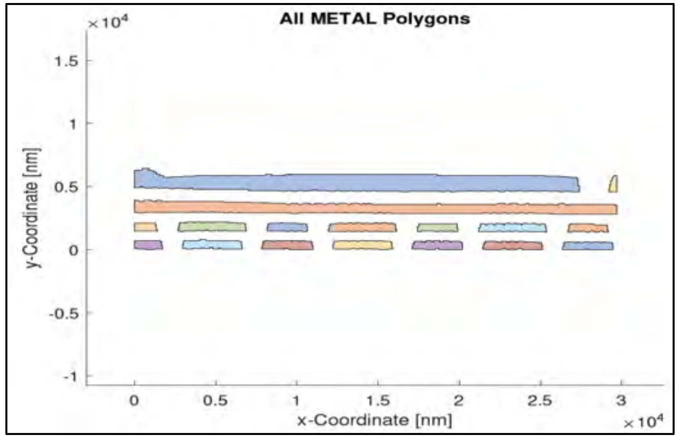
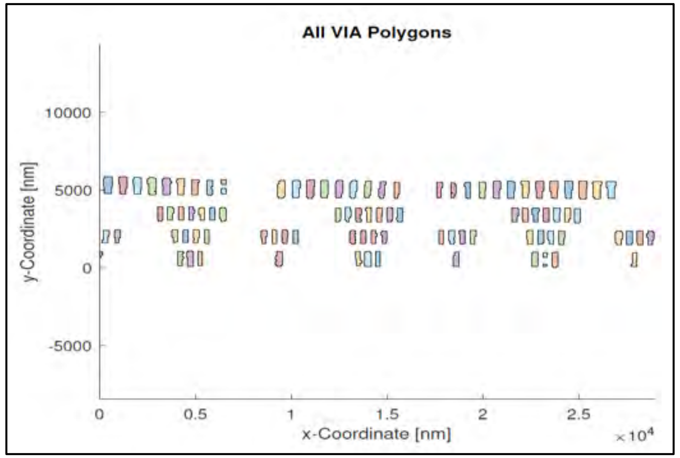


Extracted Technological Features









Synopsis and Future Work

- Outcomes
  - Approach will be used as an engineering solution for cross-section interpretation and technology inference within IFX reverse
  - Image segmentation architecture can be used for future applications with similar scare availability of data
  - Novel toolchain enabling big data processing for huge data bases that could not be handled manually
  - Newly created data-set of segmented SEM images could foster similar use-cases in the semiconductor industry
- Expected impact
  - Contribution and extension of physical hardware verification methodology
  - Step towards hardware assurance and trust via analysis capabilities
  - Contribution for fraud detection on the silicon level

Event Organisers

The Key Digital Technologies Joint Undertaking - the Public-Private Partnership for research, development and innovation – funds projects for assuring world-class expertise in these key enabling technologies, essential for Europe's competitive leadership in the era of the digital economy. KDT JU is the successor to the ECSEL JU programme. www.kdt-ju.europa.eu

The AI4DI project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 826060. The JU receives support from the European Union’s Horizon 2020 research and innovation programme and the national authorities. www.ai4di.eu

The TEMPO project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 826655. The JU receives support from the European Union’s Horizon 2020 research and innovation programme and Belgium, France, Germany, The Netherlands, Switzerland. www.tempo-ecsel.eu

The ANDANTE project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 876925. The JU receives support from the European Union’s Horizon 2020 research and innovation programme and Belgium, France, Germany, The Netherlands, Portugal, Spain, Switzerland. www.andante-ai.eu

Thank You

For your attention

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