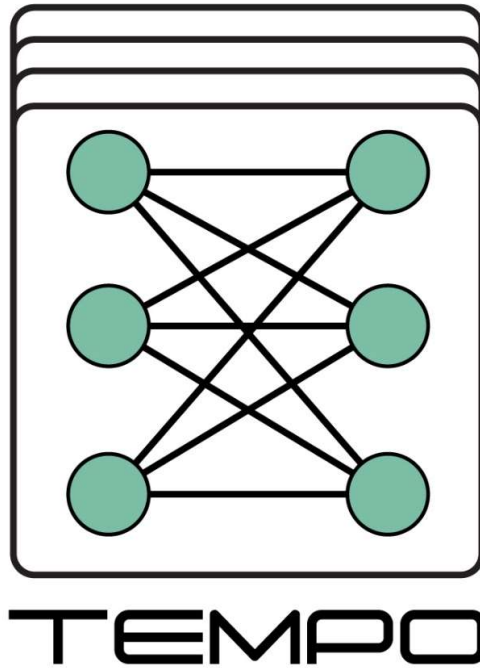


Technology & Hardware for neuromorphic computing

- ECSEL Research and Innovation Actions (RIA*) -



Deliverable 5.3

- Current Infrastructure Capabilities -

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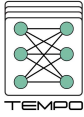
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1 Summary

The main objective of TEMPO is to build a **European eco-system** around the development, production and application of neuromorphic hardware through an **efficient cross-fertilization** between major European foundries, chip design, system houses, application companies and research partners. TEMPO is a first step in the direction of creating an implementation plan that supports the creation of a **pan-European research infrastructure** for advanced computing technologies. A major goal of the project is to bring together the world-class expertise and infrastructures of CEA (Leti), IMEC and Fraunhofer-Verbund Mikroelektronik (FHG), and together with semiconductor companies and system houses to explore the possibilities of the developed technologies.

The goal of this Work Package (#5) is “*Technology Alignment and Road-mapping*” and this D5.3 deliverable reports progresses in task T5.2 regarding the different infrastructure capabilities. Three different sections bring insights regarding the **memory technologies** themselves (process flows) in section 3, the **contamination concerns** in section 4 to allow flying wafers between the RTOs and finally the **data management** in section 5 to allow data exchanges in similar format in a near future. Different teams have been involved and the cross-fertilization is improving significantly.