This project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 826655. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Belgium, France, Germany, Netherlands, Switzerland

Addressing the call/topic: H2020 ECSEL-2018-2-RIA
Research and Innovation Action

TEMPO
Technologies and hardware for neuromorphic computing

Deliverable

D5.2 – Report on Base wafer Delivery

Work Package:	WP5 (Technology alignment and roadmapping)
Dissemination level:	Confidential
Official due date:	28.02.2022
Document editor:	Varvara Brackmann (FhG)
Contributing partners:	IMEC, CEA, FhG
Internal reviewers:	Fabrice Nemouchi (CEA), Ilja Ocket (IMEC)
Document version:	V1

1. Publishable summary

In Frame of TEMPO project, the deliverable D5.2 belongs to the work package WP5 (Technology alignment and roadmapping) and more specifically, it is the second and last deliverable of task T5.1 entitled “Define and Realize base-wafers”. Earlier in the project, the D5.1 deliverable - Designed base wafer specification - described the type of base-wafers requirement for each memory technology (MRAM, FeFET and RRAM) and the foundry selected to supply short-loops and CMOS base-wafers. Technical architectures and designs were provided to the foundry while a first set of criteria acceptance such as defectivity and contamination were reported. In D5.2 deliverable, final status of lot in WIP (Wafer In Progress) is reported. The present report is also focusing on additional acceptance criteria, potential issues that delays the demonstrators, or process development and studies realized in frame of WP5 and no reported in the WP2 or WP3 but of course are linked with.