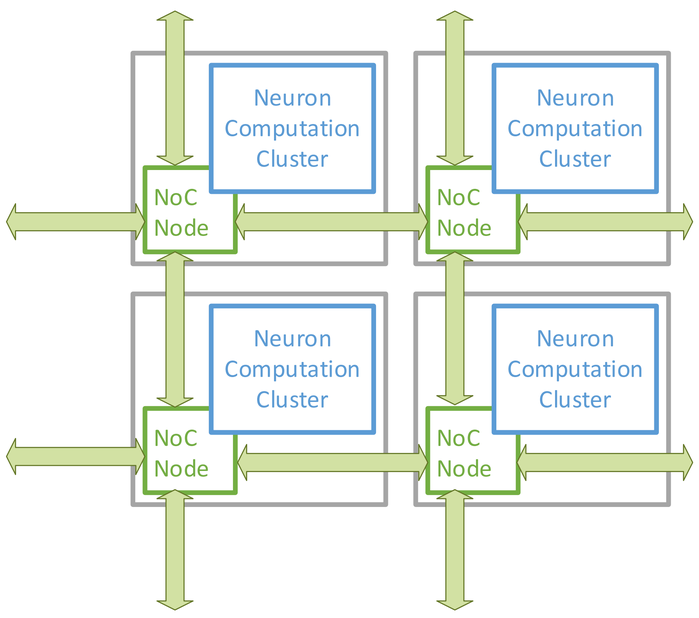
# Scalable energy efficient neuro-morphic computing architecture

***enabling platform for a diversity of SNN applications***

TEMPO

The SENeCA (Scalable Energy efficient Neuromorphic Computing Architecture) platform supports the implementation of spiking neural network application implementations over a diversity of applications and use cases within the TEMPO project and beyond.

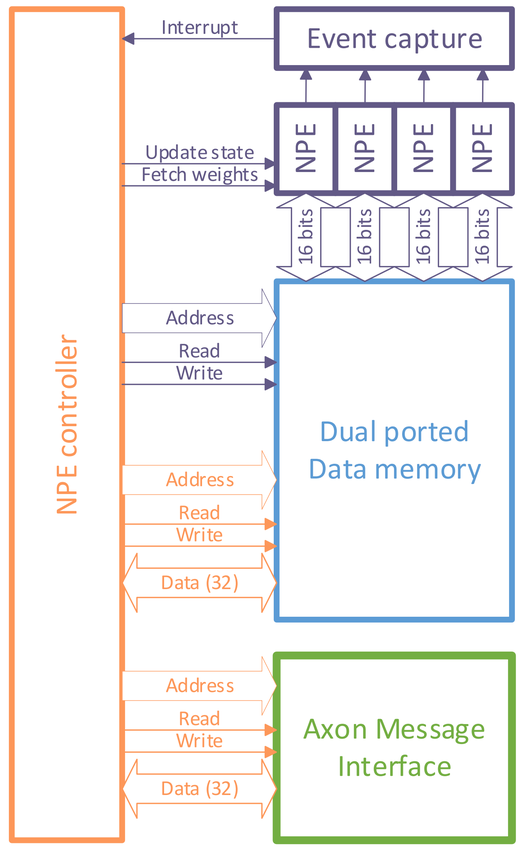
**Health**

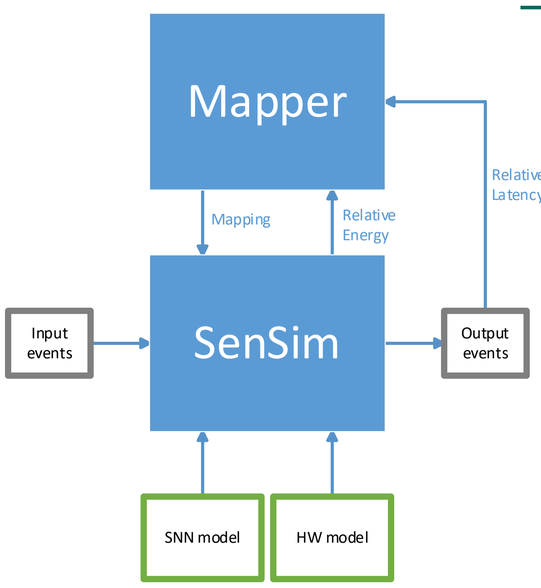



The **SENeCA** architecture consists of:

- Multiple **Neuron Computation Clusters**
- Interconnect for **event driven** communication
- **External** shared memory (for bigger applications)

- NPE controller is a **RISC-V** processor which processes the incoming axon messages and creates outgoing axon messages
- **NPE SIMD Accelerator** can do multiple Neurons in one computing cycle
- The **local memory** will contain the weights, Neuron states, interconnect tables
- The **Axon Message interface** will be connected to the interconnect to all the other NCC's
- The memory controller is the access to **shared memory** (off chip)



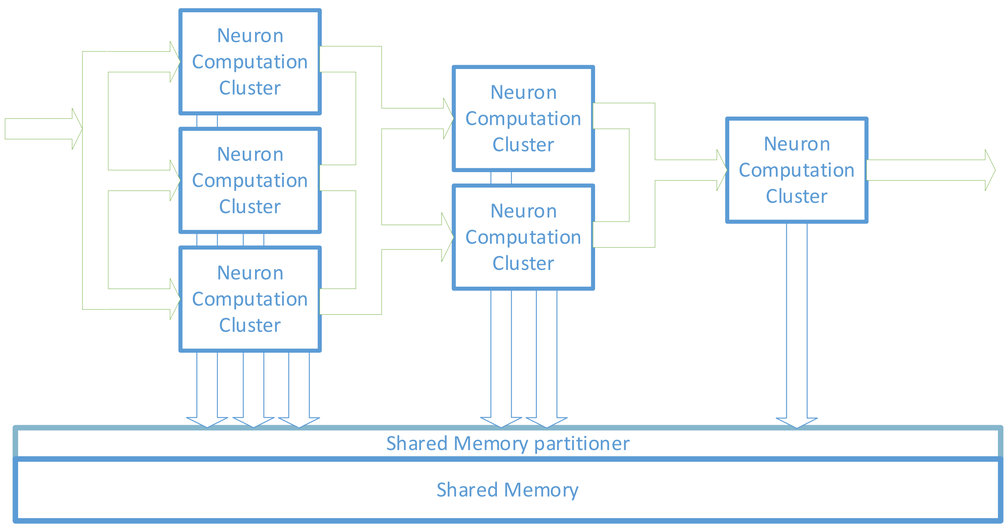

**SENeCA Simulator**

- **Provides temporal state** of cores/interconnect
- Architectural **exploration**
- **Emulation** of Scaled-up platform
- Abstract the HW for **mapping** and **application optimization**

**Mapper**

- **Optimize** resource allocations (Memory/Processing time) to Neural Network graph.

- A **possible architecture** after using the Simulator and Mapper
- Parametrizable: the **amount of NCCs**, the number of **neurons per NCC** and the **bandwidth** of the event driven interconnect




Demonstrator partners

imec

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