This project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 826655. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Belgium, France, Germany, Netherlands, Switzerland

Addressing the call/topic: H2020 ECSEL-2018-2-RIA
Research and Innovation Action

TEMPO
Technologies and hardware for neuromorphic computing

Deliverable

D5.4 – Wafer Exchange Feasibility Study

Work Package:	WP5 (Technology alignment and roadmapping)
Dissemination level:	Confidential
Official due date:	30.09.2021
Document editor:	Varvara Brackmann (FhG)
Contributing partners:	IMEC, CEA, FhG
Internal reviewers:	Fabrice Nemouchi (CEA), Ilja Ocket (IMEC)
Document version:	V1

1. Publishable summary

The central objective of TEMPO is to build a **pan-European research infrastructure** for the development, production and application of neuromorphic hardware. This infrastructure consists of institutions with world-class expertise and equipment CEA, IMEC and FhG, as well as semiconductor companies and system houses.

An essential basis for building the infrastructure between many partners is the possibility to exchange wafers to be able to benefit from each others means (equipment, processes and expertise). During the TEMPO project we analysed the requirements of each partner for the wafer exchange with external partners. We observed that there are many similarities in methods and activity management, but also some differences. It was a challenging task to align the wafer exchange procedure between the partners, and to find an agreement and unified procedure for the wafer exchange to simplify and accelerate the collaboration on the neuromorphic topics. **Contamination aspect** as well **as joint data management** were the central topics of the collaborative **wafer exchange feasibility study**. In D5.1 we described the study of the contamination criteria for base wafer exchange with the semiconductor foundries. In D5.3 we reported the comparative study of the contamination control protocols at CEA, IMEC and FhG, and proposed an alignment & common protocol exchange based on a white-list strategy.

In this deliverable D5.4 we describe our continued study on the topic of **common protocols for wafer exchange**, which includes cross-contamination check investigation (section 3.2) and alignment of the technical details (section 3.1) for the contamination control between three partners. As a result of the comprehensive cross-contamination study, we agreed on the common protocol for the future wafer exchange between CEA, IMEC, FhG and semiconductor foundries providing base wafers (section 3.7).