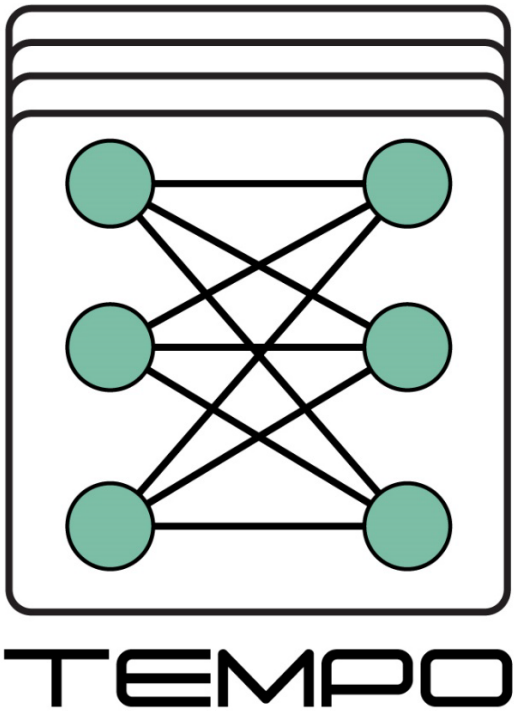
Technology & Hardware for nEuromorphic coMPuting

- ECSEL Research and Innovation Actions (RIA*) –



Deliverable 5.1
– Designed base wafer specification –

Work Package	WP 5 – Technology Alignment and Road-mapping
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1 Publishable summary

This deliverable documents the basewafer designs used for OxRAM, MRAM and FeFET based hardware in the project.

In the TEMPO project, 3 different basewafers are designed, with careful attention to how to cointegrate the different memory devices processed in CEA, Fraunhofer and imec on top of standard foundry silicon. While the deliberables in WP2 document the different test structures that are used to measure and optimize the memory devices, WP5 focuses on the logistic and process aspects required to move from foundry fabs to RTOs and in some cases back.

After a brief introduction that summarizes the eNVM building blocks designed in WP2, this deliverable documents the application targets and intent of every basewafer, the specific requirments of the various basewafers and the associated wafer acceptance criteria.