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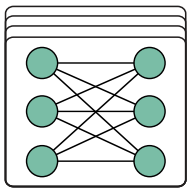

TEMPO

Technologies and hardware for neuromorphic computing

Deliverable

D4.9 - SNN Module Final Design

Work Package:	WP4 (Design and Architecture)
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1. Publishable summary

In the project Tempo, the partners IFAG, CEA, UZH and SynSense explored the neuromorphic technology of spiking neuronal networks (SNN). The results of the exploration were used by the partners to design a new generation of AI accelerators. This deliverable presents the final designs of these accelerators from IFAG, CEA, UZH and SynSense. Hence, it builds upon and extends the content of previous deliverables. The presented implementations include FPGA as well as ASIC variants. Furthermore, the partners based their accelerators on different approaches for example SynSense converts CNNs to SNNs and IFAG implements SNNs directly. Besides these details, the future steps and plans for the SNN FPGAs and ASICs are described in this deliverable as well.