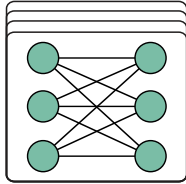




This project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 826655. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Belgium, France, Germany, Netherlands, Switzerland



Addressing the call/topic: H2020 ECSEL-2018-2-RIA  
Research and Innovation Action



# TEMPO

Technologies and hardware for neuromorphic computing

## Deliverable

### D4.9 - SNN Module Final Design

<b>Work Package:</b>	WP4 (Design and Architecture)
<b>Dissemination level:</b>	Confidential
<b>Official due date:</b>	30.11.2021
<b>Document editor:</b>	Kay Bierzynski (IFAG)
<b>Contributing partners:</b>	CEA, SynSense, UZH, IFAG
<b>Internal reviewers:</b>	Peter Debacker (IMEC), Ilja Ocket (IMEC)
<b>Document version:</b>	V1

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## 1. Publishable summary

In the project Tempo, the partners IFAG, CEA, UZH and SynSense explored the neuromorphic technology of spiking neuronal networks (SNN). The results of the exploration were used by the partners to design a new generation of AI accelerators. This deliverable presents the final designs of these accelerators from IFAG, CEA, UZH and SynSense. Hence, it builds upon and extends the content of previous deliverables. The presented implementations include FPGA as well as ASIC variants. Furthermore, the partners based their accelerators on different approaches for example SynSense converts CNNs to SNNs and IFAG implements SNNs directly. Besides these details, the future steps and plans for the SNN FPGAs and ASICs are described in this deliverable as well.