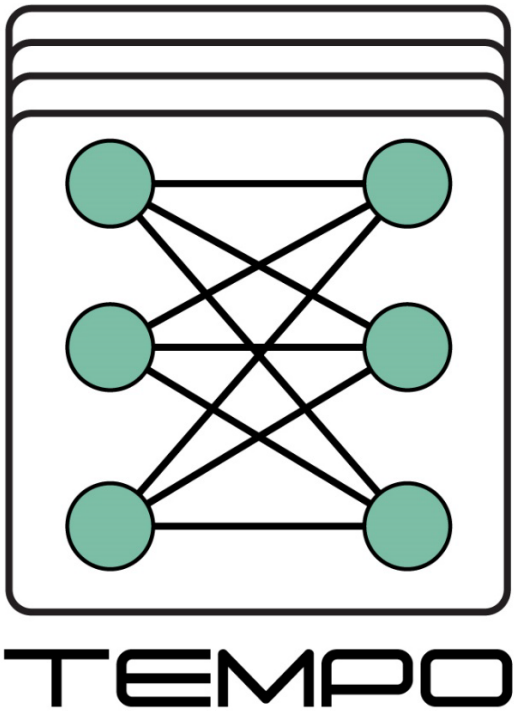
Technology & Hardware for nEuromorphic coMPuting

- ECSEL Research and Innovation Actions (RIA*) –



Deliverable 4.8
SNN Arch Design Scope

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ECSEL Joint Undertaking

1. Publishable summary

Spiking neural network (SNN) emulation accelerators developed within TEMPO are aimed at providing efficient SNN execution integrating non-volatile memories, namely memristors made using different technologies depending on the partner. These memristors are used to efficiently store network parameters in a non-volatile manner, offer high memory density and low energy consumption. They can be used in the digital domain, as a resistive RAM, or in the analog domain to emulate spiking neuron behaviours. The design of the surrounding circuit and logic depends on the way these memristors are integrated into SNN modelling. Their global architecture might also differ in order to support different coding strategies, network topologies and parameter precision.

In this deliverable, we aim to describe the architecture of SNN accelerators and the systems in which they will perform their tasks. We exhibit design choices made to model SNN mechanisms and how the obtained networks are interfaced the input from WP6.