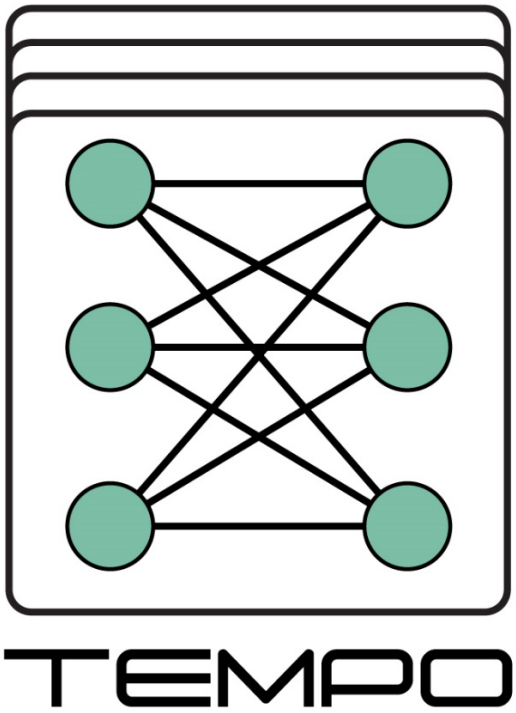
Technology & Hardware for nEuromorphic coMPuting

- ECSEL Research and Innovation Actions (RIA*) –



Deliverable 4.7
Routing Components for SNN

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ECSEL Joint Undertaking

1. Publishable summary

In this report, we explore the design space of a tree topology interconnect architecture for the neuronal fabric currently under development. This task explores the design of the interconnect to determine options for topology, topology generation and balancing, address space management, partitioning of communications flows, dimensioning of routing resources.

This exploration yielded insights into the impact of buffering and network clustering on the latency performance and resource utilization of the interconnect structure. Importantly, the study points to the importance of low-complexity interconnect strategies, even when these result in large arrays with high node counts. The outcomes of this activity will be explored in more detail as the hardware implementation matures, especially the topic of hardware costs for low-complexity (low radix) interconnects.