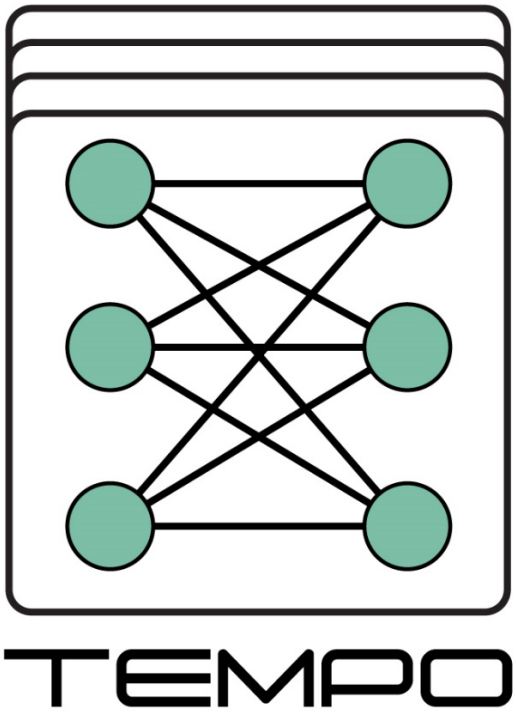
Technology & Hardware for nEuromorphic coMPuting

- ECSEL Research and Innovation Actions (RIA*) –



Deliverable 4.5
– Neuron and interface circuit designs for SNN–

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ECSEL Joint Undertaking

1. Publishable summary

Recent years have seen an increasing interest in the development of artificial intelligence circuits and systems for edge computing applications. In-memory computing neuromorphic architectures provide promising ultra-low power solutions for edge-computing sensory-processing applications, thanks to their ability to emulate spiking neural networks in real-time. The fine-grain parallelism offered by this approach allows such networks to process the sensory data efficiently by adapting their dynamics to the ones of the sensed signals, without having to resort to the time-multiplexed computing paradigm of von Neumann architectures. To reduce power consumption even further, we present a set of mixed-signal analog/digital circuits that exploit the features of advanced FDSOI integration processes. Specifically, we explore the options of advanced FDSOI technologies to address analog design issues and optimize the design of the analog DPI synapse and of the AdExp-I&F neuron circuits accordingly. We present circuit simulation results and demonstrate the circuit's ability to produce biologically plausible time constants with small capacitors and going beyond what is achievable with bulk CMOS processes and minimize power consumption, reaching figures that have at least a factor of 5_ improvement over the current state-of-the-art.
Moreover, we present a neuromorphic architecture where these components can be incorporated into a neuromorphic system with memristive devices. We present interfacing learning circuits with memristive devices based on ReRAM measurements which can be used for an online learning scenario.