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1. Publishable summary

This report describes the architectural design and modelling of the most critical building blocks of the deep neural network accelerators, with the objective to minimize their resources and the power consumption and to maximize their throughput. This work leveraged the emerging MRAM and FeFET technologies from WP2. The design and optimisation steps of several ASIC designs and hardware models are described, and optimization methodologies are presented. This work feeds the power performance area (PPA) activities performed in this project, as well as the application demonstrators.

rmann/adcsurvey.html.