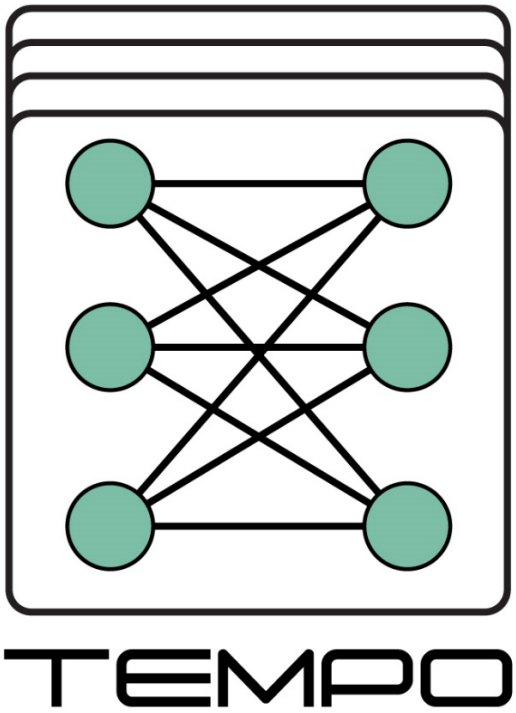
Technology & Hardware for nEuromorphic coMPuting

- ECSEL Research and Innovation Actions (RIA*) –




# Deliverable 4.2
# – Mixed-signal processing blocks for DNN –

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|---|---|
| Work Package | WP N° 4 – Design and Architecture |
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ECSEL Joint Undertaking

# 1. Publishable summary

This deliverable presents a blueprint for a 10000TOPS/W matrix-vector multiplier for neural network inference based on Analog in-Memory Computing (AiMC), an energy efficiency at least 10x beyond ultimate digital implementations. It provides: (1) a first-order analysis of a compute array with pulse-width encoded activations and a simple precharge-discharge summation line, (2) key device requirements for such a compute array, (3) examples of devices unsuited for this application (typical filamentary ReRAM and STT-MRAM), and (4) looks for a suited memory device: 2T IGZO DRAM. This compute cell and the related specs on read and write devices will drive the TFT based device optimization work in WP2.