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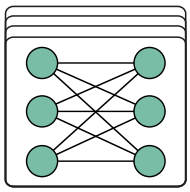

TEMPO

Technologies and hardware for neuromorphic computing

Deliverable

D4.10 – DNN 3D Module PPA

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1. Publishable summary

Analog In Memory Computing solution for DNN are being applied, but the existing solutions suffers from the significant need for on-chip memory and a huge cost of memory energy. We investigated the enablement of on-chip memory using the 3D techniques that can be scaled up for future DNN HW implementation. This deliverable reports the impact of 3D logic-memory partitioning for DNN hardware: how it can help to enable the huge data processing requirement in the DNN application domain, and what are the limitations and challenges.