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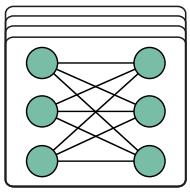

TEMPO

Technologies and hardware for neuromorphic computing

Deliverable

D3.8 – 3D PnR flow enablement

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1. Publishable summary

3D integration has traditionally been considered as one of the most promising ways to continue traditional CMOS scaling. Modern advanced SoCs are highly heterogeneous, meaning that they incorporate several subsystems within the same chip. This creates a perfect environment for 3D integration to thrive, as the very fine pitches of 3D interconnect achievable with Wafer-to-Wafer (W2W) Hybrid Bonding (HB) match the requirement for SoC breakdown into smaller functional blocks, leading to architectural optimizations. The scope of this deliverable is that of developing a full-blown design flow for the design of a three-dimensional Integrated Circuit (IC). This includes several design aspects, going from a system partitioning methodology to a 3D-aware Place and Route (PnR) flow, aided by 3D timing analysis and optimization strategies. In this report, we describe an EDA infrastructure to enhance the level of maturity of commercial tools with respect to 3D integration, enabling the physical implementation of 3D ICs. The aspects covered: 3D partitioning, place and route, and 3D timing analysis.