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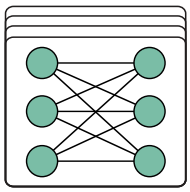

TEMPO

Technologies and hardware for neuromorphic computing

Deliverable

D3.2 – 3D RC optimization

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1. Publishable summary

3D partitioning of devices is viewed as one of the key enablers for pushing device scaling beyond the current apparent wall, implied by Moore's Law, at sub 3 nm device architecture. A key technology enabler for 3D system partitioning is the ability to connect the separate sub-parts of the SoC using die bonding techniques. RC optimisation related to 3D Heterogeneous Integration concepts primarily focus on the impact of inter-die connections reducing in pitch and wire length. In this report, we investigate how the pitch of the inter-die connections can be reduced beyond what is available in the micro-bump field. We investigate to perform either wafer-to-wafer (W2W) level or Die-to-Wafer (D2W) level hybrid bonding. Based on our investigation, we confirm that the impact of hybrid bonding on the performance is critical, especially for low power and high-performance applications. We investigated and validated different hybrid bonding techniques.