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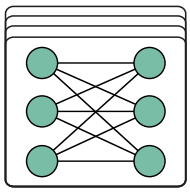

TEMPO

Technologies and hardware for neuromorphic computing

Deliverable

# D3.10 – TFT device optimization runs

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# 1. Publishable summary

$InGaZnO_4$-based thin film transistors (IGZO-TFT) are very promising for neuromorphic computing applications thanks to the low off current and BEOL compatibility [1][2]. From planar to FinFET devices, front-gated architectures are commonly used to enable high density circuits. Integrating IGZO channels in such schemes is challenging due to its high sensitivity to process conditions, including hydrogen, and scavenging at the contact areas [3][4]. To optimize each device component, we need to enable flexibility to selectively engineer them. The integration scheme is fundamental in this regard. In this report, we present the gate last (GL) integration scheme, identifying its limitations, design aspects, and effect on the electrical characteristics. We also introduce an integration module, oxygen tunnel, to locally recover defects generated in the channel. We also demonstrate the possibility to avoid the need of post processing defect recovery thanks to the channel and gate dielectric scaling. Finally, we benchmark IGZO channel materials within the same device architecture.