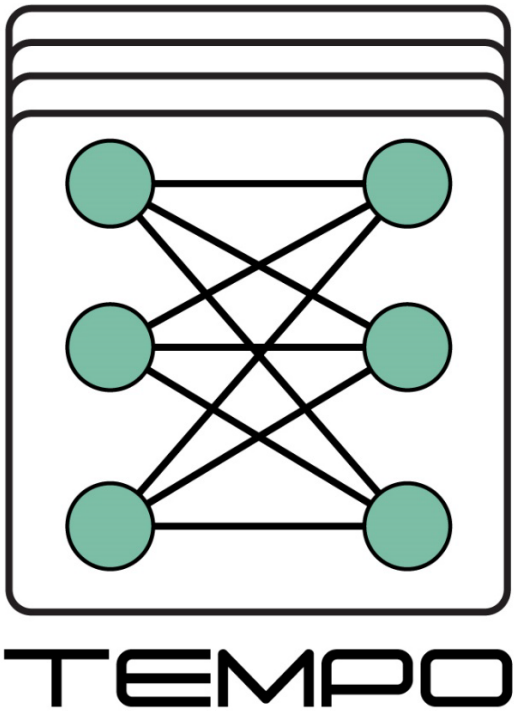
Technology & Hardware for nEuromorphic coMPuting

- ECSEL Research and Innovation Actions (RIA*) –



Deliverable 2.4
– Definition of TFT Building Blocks –

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Publishable Summary

One of the main objectives of Work Package 2 on emerging technologies is to define a set of neuromorphic building blocks that will be measured, modelled and simulated in order to find the right specifications of emerging memory devices for neuromorphic applications. To this end, test vehicles are designed in TEMPO to develop and characterize four memory technologies. This deliverable documents the TFT test vehicle and the test structures on it.

The test vehicle is meant to drive development of thin film transistors integrated in the interconnect stack and will be fully processed at imec. To this end, the vehicle contains 2 metal layers, in between which TFT devices will be placed.

The main goal is to do basic device exploration and path finding, in order to drive IGZO devices and potentially other TFT devices to short gate length, 300mm CMOS compatible transistors in the interconnect stack. Since this is still the topic of ongoing research, most test structures are at device level to be able to flexibly explore the device architecture, material stacks and the overall process integration and to characterize and model the devices that imec manufactures.

Once these devices are working well, they can be envisioned to be used in WP4, for example as a flexible and efficient communication bus between different synaptic SNN arrays.