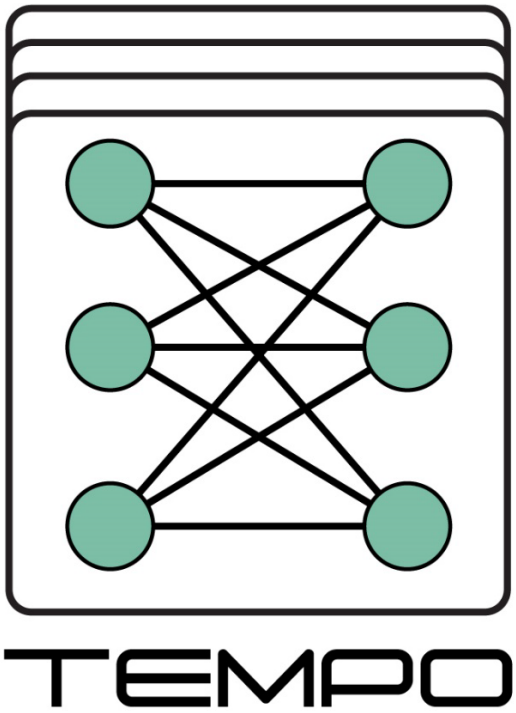
Technology & Hardware for nEuromorphic coMPuting

- ECSEL Research and Innovation Actions (RIA*) –



Deliverable 2.1
– Definition of MRAM building blocks –

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Publishable Summary

One of the main objectives of Work Package 2 on emerging technologies is to define a set of neuromorphic building blocks that will be measured, modelled and simulated in order to find the right specifications of emerging memory devices for neuromorphic applications. To this end, test vehicles are designed in TEMPO to develop and characterize four memory technologies. This deliverable document the MRAM test vehicle.

The test vehicle is based on a GlobalFoundries basewafer in 40nm LP, processed until M4. After that, the wafers will be finished at imec, where MRAM devices are added in between M4 and M5. The wafer is finished with additional metal up to M7 (though the simple test structures can be finished with M5 only).

Additionally, this deliverable describes the test structures designed on the vehicle, ranging from single 1R memory devices to megabit sized arrays and a binary NN accelerator prototype based on MRAM for weight storage (which is linked to imec's activities in WP4 on DNN design and architecture).

Finally, a brief overview is given on the STT-MRAM process flow targeted in this test vehicle.